4I36
QUADRATURE COUNTER MANUAL

1.3 for Firmware Rev AA05,BB05 or >

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GENERAL

DESCRIPTION

The 4I36 is a stackable PC/104 card with eight 32 bit up/down counters with quadrature count inputs and per channel index inputs. The 4I36 is intended for robotic, motor control, measurement, and instrumentation applications.

The 4I36 has selectable TTL or RS-422 levels on its quadrature and index inputs. TTL or RS-422 operation is jumper selectable in groups of two channels. The TTL inputs have pullup resistors and RC / Schmitt filtering. The differential RS-422 inputs are suited for longer cable lengths and have optional termination. 24 general purpose I/O bits capable of sinking 24 mA are provided control applications. The Encoder connectors are compatible with the 4I30, and the I/O connector is compatible standard I/O module racks.

The 4I36 counters can count in normal quadrature mode (4X) or up/down mode (1X). Digital filtering is used on encoder inputs to reject input noise. The 4I36 counters may cleared individually, or all counters may be cleared simultaneously. Each counter has a option to be cleared by either the rising or falling edge of the index signal. Maximum count rate of the 4I36 with TTL inputs is 4 million counts per second. Maximum count rate with RS-422 inputs is 10 million counts per second. Count range is -2,147,483,648 to +2,147,483,647 or 0 to 4,294,967,295. Any counter may be configured to provide a timing reference for velocity calculations instead of quadrature input. This timing reference is a 32 bit up counter running at 48 MHz +- .01%.

The 4I36 is a 16 bit card and uses an index register to access the many registers on the chip, the index register has an auto-increment function that allows all 8 of the 32 bit counters to be read in only 17 16 bit I/O read instructions.

The 4I36-1 is a lerger FPGA version which provides all the same base features as the 4I36 and adds the option of up to 12 PWM outputs available on the GPIO pins. These PWM outputs can be enabled separately and do not interfere with normal GPIO operation unless enabled.

The 4I36 uses a FPGA chip for all counting and I/O so can be easily upgraded or modified in the field for specific requirements. The FPGA configuration flash memory can be updated from the host, no special cable or adapters are required.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 4I36 card is oriented in an upright position, that is, with the PC/104 connector on the bottom and the white PCB markings right side up.

I/O BASE ADDRESS

The 4I36 card is an I/O mapped device that uses 8 contiguous 16 bit ports. The base address and can be located in 4 different places in the hosts I/O space. Jumpers W5 and W6 select the 4I36 base address:

W5	**W6**	**BASE ADDRESS**
DOWN	DOWN	0x220 (DEFAULT)
DOWN	UP	0x230
UP	DOWN	0x240
UP	UP	0x250

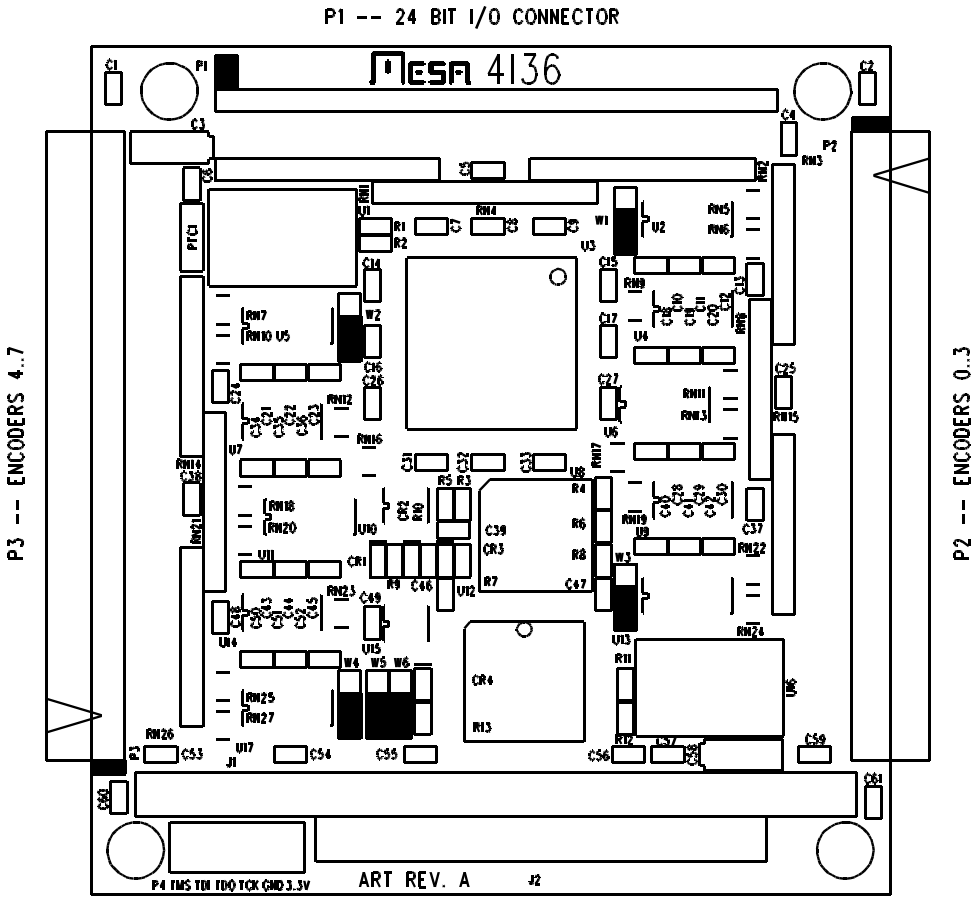
RS-422 INPUT ENABLE

The 4I36 can accept either TTL or RS-422 (differential) encoder inputs. The choice of inputs is made with jumpers W1,W2,W3, and W4. Each jumper control the input mode for 2 input channels. When a jumper is in the "UP" position, RS-422 mode is selected. When a jumper is in the "DOWN" position, TTL mode is selected. The following table shows the correspondence between mode jumpers and input channels:

W1	Controls encoder input channels 0 and 1	DEFAULT=DOWN
W2	Controls encoder input channels 6 and 7	DEFAULT=DOWN
W3	Controls encoder input channels 2 and 3	DEFAULT=DOWN
W4	Controls encoder input channels 4 and 5	DEFAULT=DOWN

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

ENCODER CONNECTORS

P2, and P3, are the 4I36's encoder connectors.. These are 50 pin box headers that mate with standard 50 conductor female IDC connectors.These pinouts match the 4I30, so the 4I36 can be used a a hardware compatible replacement for the 4I30. Note that TTL inputs connect to the /xxx inputs. The RS-422 inputs have 120 Ohm termination. The termination resistors can be removed if desired on a per-connector basis.

P2 encoder connector pinout is as follows:

P2 CONNECTOR PINOUT — ENCODERS 0 .. 3

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	QA0	2	/QA0	3	GND	4	QB0
5	/QB0	6	GND	7	IDX0	8	/IDX0
9	GND	10	+5V	11	QA1	12	/QA1
13	GND	14	QB1	15	/QB1 1	6	GND
17	IDX1	18	/IDX1	19	GND	20	+5V
21	QA2	22	/QA2	23	GND	24	QB2
25	/QB2	26	GND	27	IDX2	28	/IDX2
29	GND	30	+5V	31	QA3	32	/QA3
33	GND	34	QB3	35	/QB3	36	GND
37	IDX3	38	/IDX3	39	GND	40	+5V
41	GND	42	GND	43	GND	44	GND
45	GND	46	+5V	47	+5V	48	+5V
49	+5V	50	+5V				

CONNECTORS

ENCODER CONNECTORS

P3 CONNECTOR PINOUT – ENCODERS 4 .. 7

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	QA4	2	/QA4	3	GND	4	QB4
5	/QB4	6	GND	7	IDX4	8	/IDX4
9	GND	10	+5V	11	QA5	12	/QA5
13	GND	14	QB5	15	/QB5	16	GND
17	IDX5	18	/IDX5	19	GND	20	+5V
21	QA6	22	/QA6	23	GND	24	QB6
25	/QB6	26	GND	27	IDX6	28	/IDX6
29	GND	30	+5V	31	QA7	32	/QA7
33	GND	34	QB7	35	/QB7	36	GND
37	IDX7	38	/IDX7	39	GND	40	+5V
41	GND	42	GND	43	GND	44	GND
45	GND	46	+5V	47	+5V	48	+5V
49	+5V	50	+5V				

CONNECTORS

I/O CONNECTORS

Connector P1 is the MISC I/O connector. It provides 24 I/O bits for general purpose use. Connector P1 has a pinout that matches standard I/O module racks for convenience.

P1 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	PORTA0	2	GND	3	PORTA1	4	GND
5	PORTA2	6	GND	7	PORTA3	8	GND
9	PORTA4	10	GND	11	PORTA5	12	GND
13	PORTA6	14	GND	15	PORTA7	16	GND
17	PORTA8	18	GND	19	PORTA9	20	GND
21	PORTA10	22	GND	23	PORTA11	24	GND
25	PORTB0	26	GND	27	PORTB1	28	GND
29	PORTB2	30	GND	31	PORTB3	32	GND
33	PORTB4	34	GND	35	PORTB5	36	GND
37	PORTB6	38	GND	39	PORTB7	40	GND
41	PORTB8	42	GND	43	PORTB9	44	GND
45	PORTB10	46	GND	47	PORTB22	48	GND
49	+5V	50	GND				

OPERATION

REGISTER MAP

The 4I36 occupies 8 contiguous 16 bit I/O locations starting at the selected I/O base address. The register map is as follows:

BASE ADDRESS +0x00	INDEX REGISTER
BASE ADDRESS +0x02	COUNTER LOW REGISTER (INDEXED)
BASE ADDRESS +0x04	COUNTER HIGH REGISTER (INDEXED)
	PWM REGISTER (4I36-1 only)
BASE ADDRESS +0x06	COUNTER CONTROL REGISTER (INDEXED)
	GPIO ALT SOURCE register (4I36-1 only)
	PWM RATE register (4I36-1 only)
	IRQ rate register (4I36-1 only)
BASE ADDRESS +0x08	PORT A DATA REGISTER (index register bit 11 = 0)
	IRQ SELECT REGISTER (iindex register bit 11 = 1)
BASE ADDRESS +0x0A	PORT A DDR (index register bit 11 = 0)
	IRQ MASK REGISTER (index register bit 11 = 1)
BASE ADDRESS +0x0C	PORT B DATA REGISTER (index register bit 11 = 0)
	IRQ STATUS REGISTER (index register bit 11 = 1)
BASE ADDRESS +0x0E	PORT B DDR (index register bit 11 = 0)
	VERSION REGISTER (index register bit 11 = 1)

Note: current firmware version is 0xAA05 for 4I36 and 0XBB05 for 4I36-1. If you have an older firmware version you should update your firmware to the latest bitfile included in the 4I36 distribution zipfile. Firmware version 0xAA02 and earlier have a known bug in the index autoinc feature which will cause erratic index operation if autoinc is enabled.

OPERATION

INDEX REGISTER

To conserve I/O address space, the 4I36 uses an index register to access the 8 counters and other I/O. The index register also has various global control bits.

BIT0	CounterSel0	The three counter select bits determine which counter is accessed.
BIT1	CounterSel1	""
BIT2	CounterSel2	""
BIT5	PWM sel	if set, selects PWM generators instead of counters
BIT11	IRQRegsEna	If set, IRQ registers are available instead of I/O registers.
BIT12	GlobalHold	Holds counts of all counters if set
BIT13	GlobalClear	Holds all counters in a reset state if set
BIT14	AutoInc	Causes index register to be incremented after COUNTER HIGH register is read
BIT15	CFEN	Enables access to FPGA EEPROM (Must be 0 for normal operation)

OPERATION

COUNTER REGISTERS

The quadrature counters are read as two 16 bit words: COUNTER LOW register and COUNTER HIGH register. These are located in successive locations so that a single 32 bit input instruction can be used to read the full 32 bit count value. Before a count value can be read, the desired counter must be selected by writing the counter number into the INDEX register. When the counters are read, the host is really reading a counter latch, not the actual counter. This is to prevent the count from changing during reading, giving an erroneous result.

LATCHING THE COUNT

There are three different ways of latching the current count so that it can be read by the host.

1. Writing to the COUNTER LOW register: This will latch the currently selected counter.

2. Writing to the COUNTER HIGH register: This will latch all 8 counters at once

3. Using the LatchOnRead feature of the counter: When this feature is enabled, the currently selected counter will be automatically latched when the COUNTER LOW register is read. Note that the latching occurs at the beginning of the host read cycle, so that the COUNTER LOW value will be valid when the host accepts the data. This means only 2 read operations are needed per counter to latch and read the current 32 bit count.

USING THE INDEX AUTOINCREMENT FEATURE

If an application requires reading several counters at a time, this can be accomplished efficiently by using the autoincrement feature on the INDEX register. For example, to latch and then read all 8 counters:

Write 0x4000h to INDEX register (This enables the auto increment feature of the INDEX register and selects counter 0)

Write 0x0000 to COUNTER HIGH port (this latches all counters)

Read COUNTER LOW (low word of counter 0)

Read COUNTER HIGH (High word of counter 0 + increments INDEX)

Read COUNTER LOW(Low word of counter 1)

Read COUNTER HIGH(High word of counter 1)

(Repeat reading COUNTER LOW and COUNTER HIGH for the other 6 counters)

OPERATION

COUNTER CONTROL REGISTER

Each counter has an associated COUNTER CONTROL register. These registers control the operation of the counter. COUNTER CONTROL register bits are defined as follows:

BIT0	QA	Real time QA input (Read only)
BIT1	QB	Real time QB input (Read only)
BIT2	IDX	Real Time index input on reads, clears counter if set on a write.
BIT3	LatchOnRead	If set, counter is latched automatically before it is read.
BIT4	IndexPolarity	Determines the active edge of the Index input, if set, rising edge is detected, if clear, falling edge is detected.
BIT5	ClearOnIndex	If set, an index event will clear the counter.
BIT6	ClearOnce	If set, the ClearOnIndex bit will be cleared when an index event is detected, thus disabling the index detection logic. This allows clearing the counter on only one index event and ignoring subsequent index events.
BIT7	IndexGate	If set, conditions Index so that it is only detected when QA and QB are both high or both low (depending on ABPol). Note that this usually must be used with the ClearOnce feature, as a continuous index signal will generate multiple index events if this bit is set.
BIT8	LocalHold	If set, holds (gates) the current count
BIT9	QuadFilter	If set, increases digital filter time constant on the inputs for enhanced noise rejection. This will limit the maximum count rate to ~1.5 MHz (up/down mode) or ~6 MHz (quadrature mode)
BIT10	CounterMode	If set, counter operates in up/down mode (1X) instead of quadrature mode (4X). In up/down mode QA = clock and QB = direction (high = count up)
BIT11	AutoCount	If set, counter will count up at 48 MHz

OPERATION

COUNTER CONTROL REGISTER

BIT12 Global hold (Read only)

BIT13 Global clear (Read only)

BIT14 ABPol A and B quadrature input polarity setting for gated index feature. If ABPol is high and IndexGate is high, the index signal will be detected only when both A and B inputs are high. When ABPol is low, and IndexGate is high, the index signal will only be detected when both the A and B inputs are low.

INTERRUPT GENERATION

The 4I36 can generate interrupts when the index is detected. In addition the 4I36-1 can generate interrupts at the PWM rate or submultiples of the PWM rate Interrupt generation is controlled by 3 registers: IRQSelect, IRQMask, and IRQStatus.

INTERRUPT SELECT REGISTER

This register determines which PC/104 IRQ is generated for an interrupt event. It also controls the Tri-state drive of the interrupt pin and can mask the interrupt.

IRQ	GMASK	XX	IDRVEN	ISEL3	ISEL2	ISEL1	ISEL0

Interrupt control register bits are defined as follows:

B7 IRQ R/O Interrupt request status

B6 GMASK R/W Global interrupt mask - high to enable interrupt

B5 XX Not used

B4 IDRVEN Tri-State IRQ drive enable (high to enable)

B3--B0 ISELX Interrupt select bits

Note that do to pin limitations, only the following interrupts may be selected: 5,6,7,9,10,11,12,15

OPERATION

INTERRUPT MASK REGISTER

The interrupt mask register enables interrupts from the 8 counters. A high bit in the interrupt mask register will enable the index interrupt from the corresponding counter. Note: the IRQ Select register must be properly programmed (proper interrupt selected, IDRVEN and GMASK high) before the interrupt mask register will function. Note that the interrupt mask register is accessed as 16 bits but only the low 8 (for 4I36-1) bits are used, the upper bits are dont-care on writes and will read as 0s.

IMASK7	**IMASK6**	**IMASK5**	**IMASK4**	**IMASK3**	**IMASK2**	**IMASK1**	**IMASK0**

The 4I36-1 implements one more mask bit (IMASK8) at data bit 8 to mask the PWM rate interrupt.

INTERRUPT STATUS REGISTER

The interrupt status register serves two functions: showing which counter generated the interrupt, and allowing the host to individually clear interrupts. When read, the interrupt status register bits that are high show that the corresponding counter has generated an index interrupt. When any bit of the interrupt status register is high, (and the IRQSel is setup properly) an interrupt will be asserted on the bus. Writes to the interrupt status register will AND the data written with the contents of the register. This allows the host to clear individual bits or all bits at once depending on the data written. For example, writing 0x00FE to the interrupt status register would clear ISTAT0, while not changing any other interrupt status bits. All interrupt status bits must be cleared before returning from the interrupt service routine. Note that the interrupt mask register is accessed as 16 bits but only the low 8 bits are used, the upper 8 bits are dont-care on writes and will read as 0x00h.

ISTAT7	**ISTAT6**	**ISTAT5**	**ISTAT4**	**ISTAT3**	**ISTAT2**	**ISTAT1**	**ISTAT0**

The 4I36-1 implements one more status bit (ISTAT8) at data bit 8 which reflects the PWM rate interrupt. status.

OPERATION

I/O PORTS

The 4I36 provides 24 general purpose I/O bits. These bits are organized as two 12 bit I/O ports, PORTA and PORTB. Each I/O bit can be programmed to be an input or output, To set the input or output modes, each port has an associated Data Direction Register (DDR). When a bit in the Data Direction register is set, the corresponding bit in the port becomes an output, and when clear, the corresponding bit becomes an input. Note that at startup the DDR registers are cleared to 0x000 so that all I/O bits become inputs.

I/O PORT LEVELS AND DRIVE

The I/O bits are driven directly from the FPGA. The I/O pins are TTL compatible and can sink 24 mA. The FPGA has 3.3V I/O power so that the I/O bits will swing from 0 to 3.3V when in output mode. When in input mode, the inputs are 5V tolerant.

All I/O pins have a 3.3K pullup resistor to 5V. If 5V output swing is needed and push-pull outputs are not required, you can set PORT to 0X000, and then use the DDR register to control the outputs. When a DDR register bit is 1, the associated I/O bit will be driven low. When a DDR bit is 0, the associated I/O bit will be in inout mode so it will be pulled up to 5V.

PWM GENERATORS

The 4I36-1 version implements 12 PWM generators that connect to PORTAs GPIO bits (IO0 to IO11). The PWM generators have 10 bit resolution and have a common prescaler that allows setting the base PWM rate from below 1 Hz to ~47 KHz. Each PWM channel can be enabled individually. An enabled PWM generator drives the associated GPIO pin.

PWM OUTPUT ENABLE

Before PWM is used, the PWM generator(s) must be enabled to drive a GPIO pin. This is done by writing a ‘1' to the desired bits in the ALT SOURCE register. The ALT SOURCE register is a 12 bit register accessed at offset 6 from the base address (the COUNTER CONTROL register location) when the index register is 0x20 hex. Each ‘1' bit in the ALT SOURCE register routes the corresponding PWM generator output to the corresponding GPIO output register on port A. For example an ALT SOURCE register value of 5 would route PWM generators 0 and 2 to port A output register bits 0 and 2.

In addition to the ALT SOURCE register, the normal PORTA DDR register must have bits set corresponding to the desired PWM (and GPIO) pins that are required to be outputs. That is using the preceding example, you would need to write 5 to the PORTA DDR register also to enable the PWM outputs on GPIO bits 0 and 2.

OPERATION

PWM RATE

The PWM RATE register sets the PWM output frequency for all 12 PWM output channels. The PWM RATE register is accessed at offset 6 from the base address (the COUNTER CONTROL register location) when the index register is 0x22 hex. The PWM rate is 48MHz/1024 * PWMRATE/65536. The PWM RATE register must be programmed for the PWM outputs to work.

IRQ RATE

The 4I36-1 can generate periodic interrupts at submultiples of the PWM rate. The IRQ RATE register determines the interrupt rate. The IRQ RATE register is accessed at offset 6 from the base address (the COUNTER CONTROL register location) when the index register is 0x23 hex. The interrupt rate will be PWM rate/(IRQ RATE +1), that is a IRQ rate value of 0 will set the IRQ rate to the PWM rate (divide by 1). A IRQ RATE value of 7 would set the IRQ rate to PWM rate/8. The IRQ rate register is an 8 bit register so the maximum division ratio is PWM rate/256.

PWM VALUE

The PWM VALUE registers set the PWM output duty cycle for the associated PWM generator. The PWM value is a right justified 10 bit number. Since the PWM resolution is 10 bits, a value of 0x1ff would result in a 50% duty cycle. The PWM VALUE registers are accessed at offset 4 from the base address (the COUNT HIGH register location) when the index register is 0x20 to 0x2B hex. PWM generator 0, corresponding to GPIO pin 0 is accessed with index value 0x20, PWM generator 1, corresponding to GPIO pin 1 is accessed with index value 0x21 etc etc.

The PWM generators can be written quickly by using the auto increment feature of the index register. For example:

Write 0x4020h to INDEX register (This enables the auto increment feature of the INDEX register and selects PWM VALUE register 0)

write COUNTER HIGH (with PWM value for PWM 0)

write COUNTER HIGH (with PWM value for PWM 1)

write COUNTER HIGH (with PWM value for PWM 2)

write COUNTER HIGH (with PWM value for PWM 3)

(Repeat writing COUNTER HIGH for the other 8 PWM values)

OPERATION

FPGA CONFIGURATION

Almost all of the 4i36 logic is embedded into a single FPGA. At system reset, the FPGA configuration is loaded from an on card Flash EEPROM. This EEPROM can be re-written by the host to allow the FPGA configuration to be updated or changed. A DOS mode program SC4I36 is supplied to allow overwriting the EEPROM with a new FPGA configuration. SC4I36 is invoked as follows:

SC4I36 CONFIGFILE BASEADDRESS

Where CONFIG file is a valid 4I36 FPGA configuration file and BASEADDRESS is the 4I36 base address selected by the base address jumpers. The supplied file 4I36.BIT is the default configuration file, and can be used to restore the 4I36 to normal operation if the configuration has been modified.

NOTE: For normal operation you do not need SC4I36. Please do not use SC4I36 unless you know exactly what you are doing...

CUSTOM CONFIGURATIONS

Mesa can create custom 4I36 configurations with additional counters, interrupt generation, PWM outputs, or other specialized logic. Since this is done by altering the FPGA configuration, it is usually simple, fast, and low cost. When a new configuration is available, the new configuration file is just emailed to you.

REFERENCE

SPECIFICATIONS

POWER	**MIN**	**MAX**	**NOTES**:
POWER SUPPLY	4.5V	5.5V	
POWER CONSUMPTION:	----	300 mA	
COUNT RATE (RS-422)	10 MHz	----	
COUNT RATE (TTL)	4 MHz	----	
I/O PORT SOURCE CURRENT	-24 mA	----	2.4 VOH
I/O PORT SINK CURRENT	24 mA	----	0.4 VOL
RS-422 TERMINATION	120	120	Ohms