3X20 ANYTHING I/O MANUAL

Version 1.4

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GENERAL

DESCRIPTION

The MESA 3X20 is a tiny (2.500" x 3.250") general purpose programmable I/O module that connects to the host via cabled PCI Express. The cabled PCI Express connection allows high density I/O to be remotely located (up to ~20 feet) from the host PC. The 3X20 uses a 1M, 1.5M or 2M gate Xilinx Spartan3 FPGA for all logic, so it is truly an "Anything I/O" card. The FPGA configuration can be downloaded from the PCI Express bus side, allowing simple remote updates and creation of almost any kind of specialized I/O function. On card EEPROM configuration storage allows standalone operation if desired.

Several pre-made functions are provided, including a 144 bit parallel I/O card with six 24 bit ports, a 24 channel host based servo motor controller (HostMot2), a 8 channel micro-controller based servo motor controller (*Soft*DMC), and a 16 channel, 32 bit timer counter card capable of running at 100 MHz. VHDL source is provided for all examples.

A bus mastering PCIExpress bridge is used to support high bandwidth I/O. The 3X20 has 3 I/O banks with 48 bits each. One bank has a fixed I/O voltage of 3.3 Volts, while the other two banks have individually selectable I/O voltages of 3.3, 2.5, 1.8 or 1.5V.

HARDWARE CONFIGURATION

GENERAL

There are no hardware setup options on the 3X20 cards, but several interface I/O signals setup 3X20 operation.

REVERSABILITY

The I/O connectors on the standard 3X20 are rotationally symmetrical, allowing the 3X20 module to be installed in the motherboard in either direction. This has been done to allow the PCIE connector to face in either direction without motherboard changes. Reverse installation will swap I/O 0..71 and 72..143. Note that the MP version (PCIE through P3 option) is not reversable because the high speed PCIE connections are only routed to P3. A "/REVERSE" input is available to signal the FPGA that the module is installed in the reverse orientation.

PEX8311 EEPROM ENABLE

The PEX8311 PCIE-Local bus bridge chip is configured at power up via a serial EEPROM. If the EEPROM is somehow mis-programmed or corrupted, it can be impossible to re-write the EEPROM from the PCIE bus. To recover from this problem, The EEPROM can be temporarily disabled. When the EEPROM is disabled, the bridge chip uses its default startup register values, allowing recovery. The /EEDIS signal controls the EEPROM enable function. Normally /EEDIS is unconnected, but when EEDIS is grounded the PCIE bridges EEPROM is disabled. To fix a broken EEPROM setup, you must power up the 3X20 card with the EEPROM disabled, Enable the EEPROM when still powered, and re-write the EEPROM.

FPGA CONFIGURATION MODE

The FPGA can be automatically configured at power-up by an on-card EEPROM or can be configured via the host PCIE bus. Local EEPROM configuration storage allows the 3X20 to be used in standalone applications or application that require the FPGA card tp keep functioning even when the PCIE host is down. The CONFIGMODE pin determines the startup FPGA configuration mode. When CONFIGMODE is high, automatic configuration is selected. When CONFIGMODE is low, the 3X20 must be configure by the host via the PCIE connection.

/FORCE_ON

/FORCE_ON forces the local power supply switch on the 3X20 to be enabled. This is useful for applications where the 3X20 should not power down when the host is powered down. /FORCE_ON should only be driven low by a jumper to ground or a open drain output, never driven high. /FORCE_ON is only available on REV. C and > 3X20 cards.

HARDWARE CONFIGURATION

I/O VOLTAGE SELECT

The 3X20 has three separate I/O power supplies, with each I/O bank having 48 I/O signals. One bank has a fixed I/O voltage of 3.3V, while the other 2 banks have selectable I/O voltages. Two voltage select pins are provided for each of the banks with selectable voltages :

LEFTVS1	**LEFTVS0**	**LEFT I/O 0..47 VIO**
0	0	1.5V
0	1	1.8V
1	0	2.5V
1	1	3.3V
Left I/O 48..71	uses fixed 3.3V VIO	

RIGHTVS1	**RIGHTVS0**	**RIGHT I/O 72..119 VIO**
0	0	1.5V
0	1	1.8V
1	0	2.5V
1	1	3.3V
Right I/O 120..143	uses fixed 3.3V VIO	

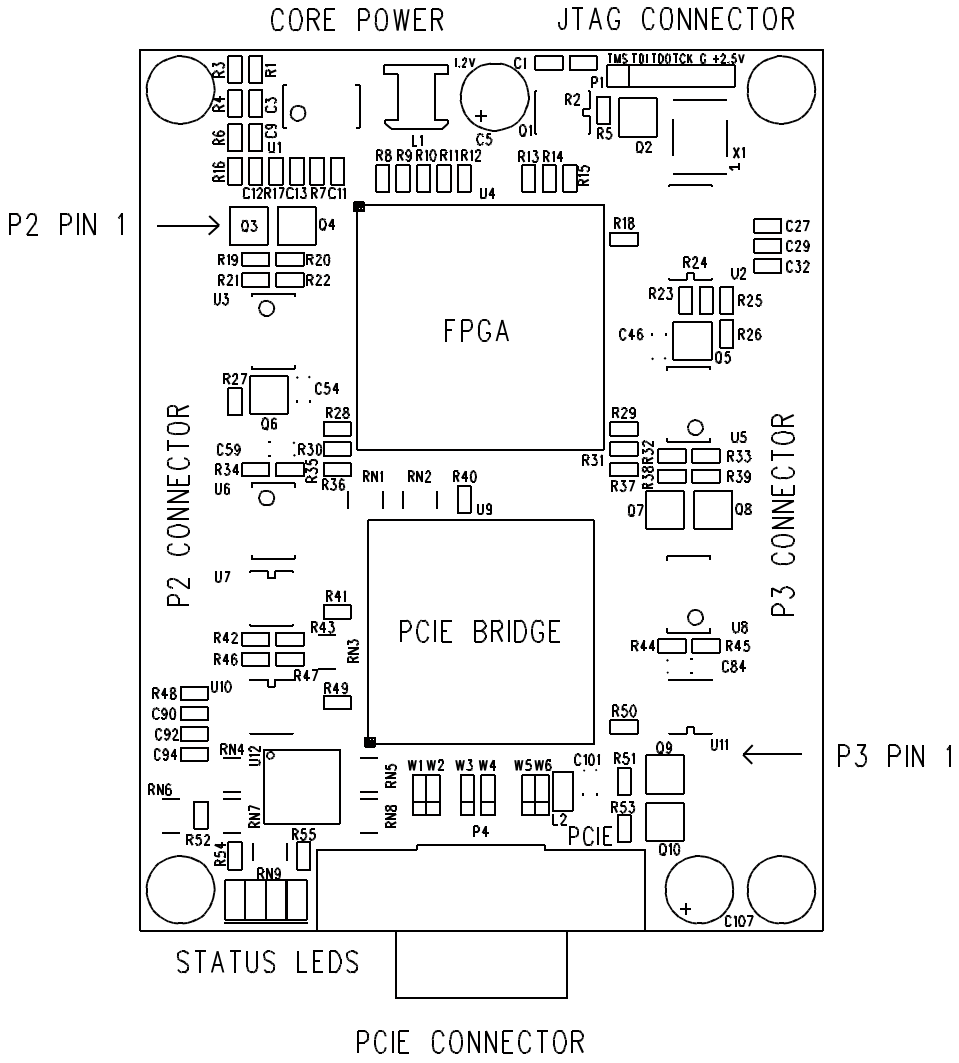
The VS pins have pulldown resistors so the I/O voltage will default to 1.5V if they are unconnected.

SWITCHED 3.3V OUTPUT

These pins supply a limited amount of 3.3V power when the 3X20 is in a power-on state. The 3.3V output pins on the 3X20 should be used as reference voltages for the CONFIGMODE and VS pins. This is so voltage is not supplied to these inputs when the 3X20 is powered down.

CONNECTORS

CONNECTOR AND MAIN CHIP LOCATIONS



CONNECTORS

I/O CONNECTORS

P2 and P3 are the 3X20s I/O connectors m outed on the bottom side of the 3X20 board. In top view, P2 is on the left hand side and P3 on the right. These are high speed board-board connectors, JAE part number WB3M200VD1T, suggested motherboard mating connector is WB3F200VD1T. Note that these connectors have 2 row, with odd pins in one row (the inner row) and even pins in the other row. For information on which I/O pin connects to which FPGA pin, please see the 3X20IO.PIN file on the 3X20 distribution zip file. 3X20 IO connector pinouts are as follows:

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
1	GND	2	GND
3	RESV	4	RESV
5	RESV	6	RESV
7	GND	8	GND
9	RESV	10	RESV
11	RESV	12	RESV
13	GND	14	GND
15	RESV	16	RESV
17	RESV	18	RESV
19	GND	20	GND
21	RESV	22	RESV
23	RESV	24	RESV
25	GND	26	GND
27	RESV	28	RESV
29	RESV	30	RESV

CONNECTORS

I/O CONNECTORS

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
31	GND	32	GND
33	RESV	34	RESV
35	RESV	36	RESV
37	GND	38	GND
39	LEFTVS0	40	LEFTVS1
41	3.3V	42	3.3V
43	GND	44	GND
45	IO0	46	IO2
47	IO1	48	IO3
49	GND	50	GND
51	IO4	52	IO6
53	IO5	54	IO7
55	GND	56	GND
57	IO8	58	IO10
59	IO9	60	IO11
61	GND	62	GND
63	IO12	64	IO14
65	IO13	66	IO15
67	GND	68	GND

CONNECTORS

I/O CONNECTORS

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
69	IO16	70	IO18
71	IO17	72	IO19
73	GND	74	GND
75	IO20	76	IO22
77	IO21	78	IO23
79	GND	80	GND
81	IO24	82	IO26
83	IO25	84	IO27
85	GND	86	GND
87	IO28	88	IO30
89	IO29	90	IO31
91	GND	92	GND
93	IO32	94	IO34
95	IO33	96	IO35
97	GND	98	GND
99	IO36	100	IO38
101	IO37	102	IO39
103	GND	104	GND
105	IO40	106	IO42

CONNECTORS

I/O CONNECTORS

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
107	IO41	108	IO43
109	GND	110	GND
111	IO44	112	IO46
113	IO45	114	IO47
115	GND	116	GND
117	IO48	118	IO50
119	IO49	120	IO51
121	GND	122	GND
123	IO52	124	IO54
125	IO53	126	IO55
127	GND	128	GND
129	IO56	130	IO58
131	IO57	132	IO59
133	GND	134	GND
135	IO60	136	IO62
137	IO61	138	IO63
139	GND	140	GND
141	IO64	142	IO66
143	IO65	144	IO67

CONNECTORS

I/O CONNECTORS

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
145	GND	146	GND
147	IO68	148	IO70
149	IO69	150	IO71
151	GND	152	GND
153	RESV	154	RESV
155	RESV	156	RESV
157	GND	158	GND
159	RESV	160	RESV
161	RESV	162	RESV
163	GND	164	GND
165	RESV	166	RESV
167	RESV	168	RESV
169	GND	170	GND
171	RESV	172	RESV
173	RESV	174	RESV
175	GND	176	GND
177	RESV	178	RESV
179	/REVERSE	180	RESV
181	3.3VIN	182	3.3VIN

CONNECTORS

I/O CONNECTORS

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
183	PWRGD	184	DONE
185	CFMODE	186	/EEDIS
187	3.3VIN	188	3.3VIN
189	RESV	190	RESV
191	RESV	192	RESV
193	3.3VIN	194	3.3VIN
195	RESV	196	RESV
197	/FORCEON	198	RESV
199	3.3VIN	200	3.3VIN

Signals marked RESV are reserved for future use and should be left unconnected on the 3X20 motherboard.

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	
1	GND	2	GND	
3	PERN0	4	PETN0	Note: P3 PCIE connections on
5	PERP0	6	PETP0	MP model only
7	GND	8	GND	
9	RESV	10	RESV	
11	RESV	12	RESV	
13	GND	14	GND	
15	RESV	16	RESV	
17	RESV	18	RESV	
19	GND	20	GND	
21	RESV	22	RESV	
23	RESV	24	RESV	
25	GND	26	GND	
27	REFCLKN	28	RESV	Note: P3 PCIE connections on
29	REFCLKP	30	RESV	MP model only

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
31	GND	32	GND
33	/CPERST	34	/CPRSNT
35	CPWRON	36	/CWAKE
37	GND	38	GND
39	RIGHTVS0	40	RIGHTVS1
41	3.3V	42	3.3V
43	GND	44	GND
45	IO72	46	IO74
47	IO73	48	IO75
49	GND	50	GND
51	IO76	52	IO78
53	IO77	54	IO79
55	GND	56	GND
57	IO80	58	IO82
59	IO81	60	IO83
61	GND	62	GND
63	IO84	64	IO86
65	IO85	66	IO87
67	GND	68	GND
69	IO88	70	IO90

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
71	IO89	72	IO91
73	GND	74	GND
75	IO92	76	IO94
77	IO93	78	IO95
79	GND	80	GND
81	IO96	82	IO98
83	IO97	84	IO99
85	GND	86	GND
87	IO100	88	IO102
89	IO101	90	IO103
91	GND	92	GND
93	IO104	94	IO106
95	IO105	96	IO107
97	GND	98	GND
99	IO108	100	IO110
101	IO109	102	IO111
103	GND	104	GND
105	IO112	106	IO114
107	IO113	108	IO115
109	GND	110	GND

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
111	IO116	112	IO118
113	IO117	114	IO119
115	GND	116	GND
117	IO120	118	IO122
119	IO121	120	IO123
121	GND	122	GND
123	IO124	124	IO126
125	IO125	126	IO127
127	GND	128	GND
129	IO128	130	IO130
131	IO129	132	IO131
133	GND	134	GND
135	IO132	136	IO134
137	IO133	138	IO135
139	GND	140	GND
141	IO136	142	IO138
143	IO137	144	IO139
145	GND	146	GND
147	IO140	148	IO142
149	IO141	150	IO143

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
151	GND	152	GND
153	RESV	154	RESV
155	RESV	156	RESV
157	GND	158	GND
159	RESV	160	RESV
161	RESV	162	RESV
163	GND	164	GND
165	RESV	166	RESV
167	RESV	168	RESV
169	GND	170	GND
171	RESV	172	RESV
173	RESV	174	RESV
175	GND	176	GND
177	RESV	178	RESV
179	RESV	180	RESV
181	3.3VIN	182	3.3VIN
183	RESV	184	RESV
185	RESV	186	RESV
187	3.3VIN	188	3.3VIN
189	TMS	190	TDO

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC
191	TDI	192	TCK
193	3.3VIN	194	3.3VIN
195	2.5V	196	2.5V
197	RESV	198	RESV
199	3.3VIN	200	3.3VIN

DIFFERENTIAL PAIRS

The 3X20 supports LVDS signaling on all pairs of the P2 and P3 I/O connectors that have a selectable I/O voltage (The Spartan3 does not support differential signaling with 3.3VIO). The even I/O numbers are the negative half of the pair and odd I/O numbers are the positive half. For example, the first differential pair is I/O0 and I/O1. These signals are connected to the FPGA with 100 ohm impedance differential traces on the 3X20 PCB. Note that when LVDS is used, VCCIO must be set to 2.5V. All pairs are length matched so the the PCB delays add less than 50 pS to the pair-pair skew.

CONNECTORS

JTAG CONNECTOR

The 3X20 has a JTAG header location (6 pin 2mm single row). This header location can be used for JTAG access to the FPGA and CPLD. JTAG signals are 2.5V levels, and a 2.5v reference pin is provided on the JTAG connector. P1 is the JTAG connector. P1 pinout is as follows:

PIN	SIGNAL	PIN	SIGNAL
1	TMS	4	TCK
2	TDI	5	GND
3	TDO	6	2.5V

The JTAG signals are also available on motherboard connector P3.

PCIE CONNECTOR

The PCIE connection is a standard one lane endpoint connector, Molex PN 74960-3018. The PCIE connector is P4. P4 pinout is as follows:

PIN	SIGNAL	PIN	SIGNAL
A1	PERN0	B1	GND
A2	PERP0	B2	RESV
A3	RESV	B3	/CWAKE
A4	GND	B4	/CPRSNT
A5	CREFCLKN	B5	GND
A6	CREFCLKP	B6	3.3V
A7	GND	B7	CPWRON
A8	/CPERST	B8	PETN0
A9 `	GND	B9	PETP0

OPERATION

FPGA

The 3X20 use a Xilinx Spartan-III 1M, 1.5M, or 2M gate FPGA in a 456 BALL BGA package: XC3S1000-FG456, XC3S1500-FG456, or XC3S2000-FG456

FPGA PINOUT

The local bus and I/O interface FPGA pinouts are described in the 3X20INFC.PIN and 3X20IO.PIN files in CONFIGS directory of the distribution disk. The 3X20IO.PIN file may be used as a template for custom configurations. The .ucf files included with the VHDL example source are also a good reference of FPGA pinout.

MEMORY AND I/O REGIONS

The PLX8311 PCI bridge local configuration registers can be accessed via I/O or memory. These are used to setup the PCI bridge, and for manipulating the I/O bits when configuring the FPGA.

BAR	**MEM - I/O**	**WIDTH**	**RANGE**
BAR 0	MEMORY	32 BITS	128 BYTES
BAR 1	I/O	32 BITS	128 BYTES

The PLX8311 PCI bridge allows for 2 separate memory and I/O regions to be mapped to the local bus that connects to the FPGA. The default EEPROM configuration sets these up as follows:

BAR	**ADDRESS SPACE**	**MEM - I/O**	**WIDTH**	**RANGE**
BAR 2	0	I/O	32 BITS	256 BYTES
BAR 3	1	MEMORY	32 BITS	64K BYTES

LOCAL BUS INTERFACE

The 3X20 uses the multiplexed local bus option of the PLX8311 bridge chip to save FPGA pins. Because of this multiplexed bus, the FPGA interface logic must latch the LAD bus when ADS is active to create an internal address.

OPERATION

BITFILE STARTUP OPTIONS

In order to avoid a local bus lockup during the transition from an unconfigured FPGA state to a configured FPGA state, the bitfile startup options must set to the following order:

4 Release write enable

5 Enable Outputs

6 Assert Done

HOST CONFIGURATION

Before the 3X20 can do anything useful it must have its FPGA configuration data loaded. Configuration data can be loaded either from the on card EEPROM or from the host CPU. Host FPGA configuration is done by writing a series of bytes from the configuration file to the 3X20 card's configuration data register. Configuration data is written a byte at a time (right justified byte in 32 bit word) to any of the I/O or memory bus space regions mapped to the 3X20s local bus. The FPGA configuration control bits must be manipulated before configuration data can be sent to the FPGA. These control bits are controlled via GPIO pins of the PEX8311 PCIE bridge. The PEX8311s GPIO pins are connected to the following FPGA configuration pins:

GPIO	**DIRECTION**	**FPGA**
GPI	IN	DONE
GPO	OUT	/PROGRAM

EEPROM CONFIGURATION

For stand-alone applications and when it is not desired to have to preconfigure the FPGA via the host interface at power up, the 3X20 can be configured via its serial EEPROM. Of course the Serial EEPROM must first be programmed with the desired configuration file. The serial EEPROM used is a ST M25P80 SPI flash serial EEPROM.

All access the serial EEPROM is via the FPGA, so programming the serial EEPROM is a "bootstrap" process, where the first step is programming the FPGA with a configuration giving host (PCIE) access to the serial EEPROM through the FPGA. The IOPR24 demo configuration allows this EEPROM access via a simple SPI interface built into the configuration.

The FPGA will be loaded from the serial EEPROM if the CONFIGMODE pin is held high at power-up or board reset. Once configured the FPGA can be reconfigured via the PCIE host interface if desired, regardless of the CONFIGMODE setting.

OPERATION

SC3X20

A DOS utility program SC3X20.EXE is provided to send configuration files to the 3X20. The Pascal and C source for this program is available on the distribution disk, and can be used as an example for writing a custom version of download software. SC3X20 is invoked with the FPGA configuration file and the 3X20 configuration base address on the command line:

```
SC3X20 FPGAFILE.BIN
```

SC3X20 uses binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC3X20 utility sends PROM files directly to the 3X20. BIT files have their headers stripped and are bit reversed before being sent to the 3X20.

SCM3X20

SCM3X20 is a similar utility that programs the serial EEPROM on the 3X20. I has the same command line syntax as SC3X20:

```
SCM3X20 FPGAFILE.BIN
```

The SCM3X20 program relies on IOPR24 configuration file being preloaded into the FPGA before writing the serial EEPROM, as the serial EEPROM can only be accessed through the FPGA.

SC9056W

Another utility SC9056W is provided for Windows 2000 and Windows XP. This utility requires the PLX9056.SYS driver and PLXAPI.DLL API SHIM to work. The source for SC9056W can be used as an example of how to access the configured 3X20 cards under Windows 2K,XP or Vista. SC9056W is a console utility and must be run from the command line:

```
SC9056W SOMEBITFILE.BIT CARD#
```

SCM9056W

SCM9056W is a similar utility that programs the serial EEPROM on the 3X20. It has the same command line syntax as SC3X20W:

```
SCM9056W SOMEBITFILE.BIT CARD#
```

SC3X20 , SC9056W, SCM3X20, and SCM9056W use binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The utilities send PROM files directly to the 3X20. BIT files have their headers stripped and are bit reversed before being sent to the 3X20.

OPERATION

CLOCK SIGNALS

The FPGA has one on card clock source and 4 available clock inputs. The on card clock is 50 MHz routed to GCLK2. This clock functions both as the FPGA system clock and the local bus interface clock. IOBITS 0 and 1 (connector P2) are FPGA GCLK7 and GCLK6 respectively. This pair of clocks can also be used as a single LVDS differential input clock. IOBIT 142 (connector P3) is GCLK5, and IOBIT 143 (connector P3) is GCLK4.

LEDS

The 3X20 has 4 status LEDs on the bottom left edge of the card. Status signal monitored are from left to right (CR1 through CR4):

CR1	PCIE Link OK	On for Link OK
CR2	FPGA /INIT	On for FPGA reset/CRC error
CR3	FPGA DONE	On when FPGA not configured
CR4	FPGA PROGRAM	On when FPGA /PROGRAM is asserted

CR2 can be controlled by the FPGA once the FPGA is configured.

IO LEVELS

The FPGA used on the 3X20 is a Spartan3. The Spartan3 supports many I/O standards. VIO for I/O 48..71 and I/O120..143 are fixed at 3.3V so only 5 I/O options can b used with these I/O pins: LVTTL, LVCMOS_33, LVDCI_33, and LVDCI_33_DV2 . The other I/O pins will can be used with any I/O option that does not require reference pins.

Even with 3.3V VIO selected, the Spartan3 FPGA chip used on the 3X20 is not 5V tolerant, so take care when interfacing to 5V logic. The 7I68 motherboard routes the 3X20s I/O pins through bus switches that allow 5V inputs.

STARTUP I/O VOLTAGE

After power-up or system reset and before the the FPGA is configured, built in FPGA pull-up resistors will pull all I/O signals to a high level. If the FPGA is used for motion control or controlling devices that could present a hazard when enabled, external circuitry should be designed so that this initial state results in a safe condition.

OPERATION

TERMINATION

The FPGAs used on the 3X20 support series and parallel termination that can be programmed on a pin-for-pin basis. This feature is called DCI. The 3X20 supports DCI on all I/O pins. The DCI reference resistors are all 100 Ohm 1%.

POWER SUPPLY

The 3X20 runs from 3.3V power supplied via the board-board connectors. This power is labeled 3.3VIN on the connector pinout. The 3X20 uses an on card switching regulator to supply the 1.2V CORE core power for the FPGA. A maximum of 3A of core power can be supplied. Linear low dropout regulators are used for the switchable VIO. Because or the liners per bank regulators, maximum per bank VIO current depends on VIO. Maximum total 3X20 power consumption is 7 watts. Typical power consumption is approximately 3 Watts.

POWER SWITCHING

The 3X20 switches its primary 3.3V power based on the state of the PCIE signal CPWRON. This is designed to the 3X20 will power up at the same time as the host, and so that PCIE hosts that have power control capability can power down the 3X20. This feature can be disabled by grounding the /FORCEON pin.

PCIE ROUTING OPTION

The 3X20 can be supplied without the cabled PCIE connector and with its PCIE signals routed through the board-board connector for applications that have PCIE available on the motherboard. Note that the low speed PCIE signals are always available on P3, the routing option just connects the high speed PCIE signals (PETP0, PETN0, PERP0, PERN0, REFCLKP, REFCLKN) to P3.

PCIE CABLES

Standard 1 lane PCIE cables are used to connect the 3X20 to the host. MESA can supply the cables or they can be obtained through most electronic distributers. Part numbers of some representative Molex cables are as follows:

LENGTH	**PART NUMBER**
0.5 meter	74576-0000
1 meter	74576-0001
3 meter	74576-0003
7 meter	74576-0007

OPERATION

CABLED PCIE HOST ADAPTERS

Mesa currently supplies 2 host adapters that allow standard desktop computers to connect to a PCIE cable. There is a adapter for PCI hosts (5I71) and PCIE hosts (6I71) Where there is a choice, the 6I71 is preferable as it will result in lower latency and higher throughput. Third party vendors supply Express card adapters, allowing the 3x20 to be connected to a laptop Express card slot.

7I68 MOTHERBOARD

The 7I68, a 3X2X breakout motherboard is available for testing the 3X20 and for applications that wish to use Mesas' standard Anything I/O pinout connectors. The 7I68 wires the 144 I/O signals on the 3X2X to six 50 pin .1" headers with Mesas Anything I/O pinout. The 7I68 also has bus switches in series with each I/O line to provide 5V tolerance to the 3X20s I/O signals. A 5V to 3.3V regulator is also provided. The 7I68 can optionally be assembled with a PCIE connector for use with the 3X20-MB.

6I68 MOTHERBOARD

The 6I68 is another 3X2X breakout motherboard. It is basically the same as the 7I68 but is a standard 1 lane PCIE card that plugs into a PC motherboard PCIE slot.

LATENCY, TRANSFER RATES AND DMA

The bridge chip used on the 3X20 (PEX8311) is actually 2 bridge chips in a single package, a PEX8111 PCIE to PCI bridge and a PCI9056 PCI to local bus bridge. If the host interface includes a bridge (say a 5I71), the PCIE communication channel ends up with at least 3 bridges in series. This results is per transfer overheads in the 1-3 usec region. This means that bulk transfers will be dismally slow if single word-at-a-time access is used. To get reasonable transfer rates, either bus master or DMA driven transfers should be used.

The PCI9056 bridge includes a powerful and easy to use DMA controller that allows the 3X20 to support transfer rates to the 100M byte/second range. Its is suggested that high performance designs use the DMA controller. Bus master transfers are another way to reach high transfer rates, but result in a more complicated FPGA design.

SUPPLIED CONFIGURATIONS

IOPR24

The IOPR24 configuration creates a simple 144 bit parallel I/O port. IOPR24 is 32 bit device, all accesses read or write 32 bit words. IOPR24 creates six 24 bit ports. Each I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. The IOPR24 configuration also contains a simple SPI interface to provide access to the 3X20s FPGA configuration EEPROM. For information on the register map of the IOPR24 configuration, see the regmap file in the /configs/IOPR24 directory of the 3X20 distribution disk.

IOPR24-7

The IOPR24-7 configuration is a variant or IOPR24 with a pinout that matches the 7I68 motherboard, creation six 24 bit I/O ports that match the si 50 pin I/O port connectors no the 7I68.

3X20LOOP

The IOPR24 configuration provides a simple way to check that all the I/O pins are OK and that most of the host interface is working. A loopback program (3X20LOOP) is provided for doing this testing. 3X20LOOP depends on having the 3X20 installed in a 7I68 motherboard and having the an external loopback cable between I/O connectors P4, P5, and P6,P7,P8, and P9. 3X20LOOP perform a rotating bit test with one I/O connector programmed as outputs and the other two as inputs. All combinations of inputs and outputs are tested. In addition, a 32 bit register readback test is performed to verify 32 bit local data bus functionality. NOTE: all VIO must be 3.3V when ding loopback testing or the 3X20 could be damaged.

HOSTMOT2

The HOSTMOT2 configuration is a up to 16 channel host based servo motor or step motor controller. Host based controllers depend on the host CPU to "close" the servo loop. This has advantages and disadvantages. One advantage is that less hardware is needed, since host based software does all the math and handles all the control bits. Another advantage is that since the host based software is easily examined and modified, it is more amenable to customization and is more useful as a teaching tool. One disadvantage is that host based motor controllers depend on fast interrupt response time or high speed threads, since the control loop is a time critical task. This means that host based motor controllers don’t tend to work well with multitasking operating systems such as Windows or Unix. They will work with real-time operating systems or simple operating systems like DOS.

SUPPLIED CONFIGURATIONS

HOSTMOT2

HOSTMOT2 is available in several configurations the vary the number of servo or step generator channels, plus miscellaneous I/O options including 32 bit buffered UARTs, SPI interfaces, SSI interfaces etc.

The HostMot2 interface is supported by the open source EMC2 CNC control software.

*SOFT*DMC

The *Soft*DMC configuration creates a 4 or 8 axis processor based servo motor controller, with the processor embedded in the FPGA. The *Soft*DMC configuration has the advantage that the embedded processor takes care of all time critical functions, so it can control motor position and motions without host intervention.

The *Soft*DMC configuration has programmable sample and PWM rates, and can operate 4 axis at up to 50 KHz sample rate and 8 axis at up to 25 KHz sample rate.

The control loop is a PID+F loop (F=feedforward) with 16 bit tuning parameters. Position and Velocity use 32 bit parameters for wide range.

The profile generator supports position,velocity, and homing modes. Position mode includes ramp-up, slew, ramp-down motions. Velocity mode supports breakpoints and a linked list parameter loading system for accurate profiling. Profile generator uses 48 bit accumulator to allow velocities from 2 turns per day (500 line - 2000 count encoder, 4 KHz sample rate) to 60,000 RPM.

There is a separate manual available for the *Soft*DMC motion controller.

Demo programs, and tuning program (dmctune.exe) and sources are located in the /configs/softdmc/support directory of the 3X20 distribution disk.

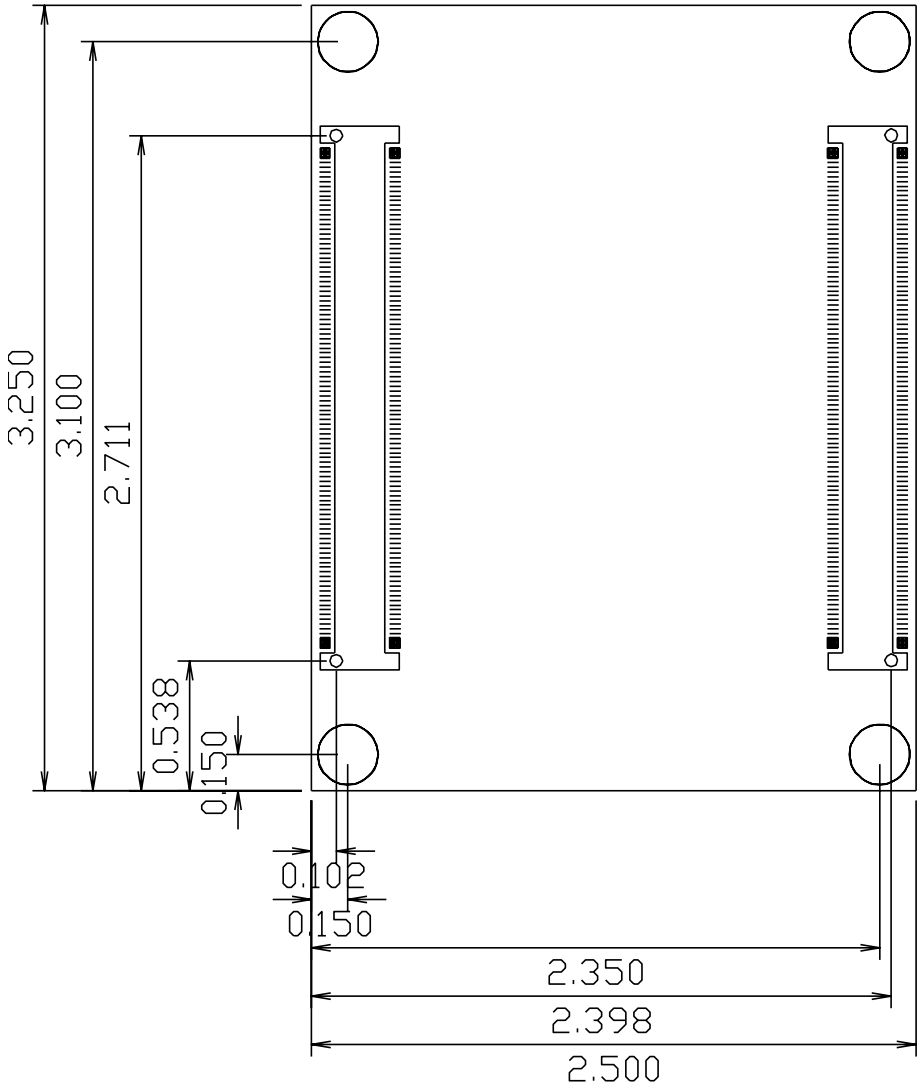
REFERENCE

SPECIFICATIONS

POWER	**MIN**	**MAX**	**NOTES**:
POWER SUPPLY	3.15V	3.45V	3.3V 5%
VIO CURRENT AT 3.3V VIO	----	1A	Per bank
VIO CURRENT AT 2.5V VIO	----	625mA	Per bank
VIO CURRENT AT 1.8V VIO	----	333mA	Per bank
VIO CURRENT AT 1.5V VIO	----	277mA	Per bank
FPGA 1.2V CORE CURRENT	----	3A	
3.3V POWER CONSUMPTION:	----	3.5A	Depends on FPGA Configuration and external load. Board power dissipation should be limited to 7 Watts
PCIE	----	GEN 1	2.5 Gbps
PCIE CABLE LENGTH	----	7	Meters
(Mesa host adapter used)			
TEMPERATURE RANGE -C version	0 ^{o}C	+70 ^{o}C	
TEMPERATURE RANGE -I version	-40 ^{o}C	+85 ^{o}C	

REFERENCE

MOTHERBOARD FOOTPRINT



Note the Motheboard connector footprints should NOT use the suggested locating pin hole sizes but rather .040" holes. This is because the connector to connector distance is critical. The suggested locating hole sizes are only appropriate for single connector use.