4I38
ANYTHING I/O
MANUAL

V1.1

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GENERAL

DESCRIPTION

The MESA 4I38 is a general purpose programmable I/O card for the PC/104 bus. The 4I38 uses a 1M or 1.5M gate Xilinx FPGA for all logic, so it is truly an "Anything I/O" card. The FPGA is downloadable from the PC/104 bus side, or from an on card serial EEPROM allowing creation of almost any kind of specialized I/O function, even including micro-controllers in the FPGA. Master (CPU replacement) mode is supported. Control of all interrupts and DMA lines make the 4I38 suitable as a PC/104 test fixture.

Several pre-made functions are provided, including a 8 channel host based servo motor controller, a 8 channel micro-controller based servo motor (SoftDMC), and a 8 channel, 32 bit timer counter card capable of running at 100 MHz. VHDL source is provided for all examples.

The 4I38M uses two 50 pin connectors with I/O module rack compatible pinouts and interleaved grounds.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 4I38/4I38M card is oriented in an upright position, that is, with the PC/104 connectors towards the person doing the configuration.

CONFIGURATION I/O DECODE

The FPGA chip that is the heart of the 4I38 is based on static RAM technology. This means that at power up or after a reset the FPGA is empty and must be configured to do whatever specific task is required of it. This configuration information is sent to the over the PC/104 bus as a sequence of bytes. The I/O location where these bytes are sent is selected by 2 jumpers on the 4I38 card, W4 and W5. The following table shows the standard I/O addresses:

W4	**W5**	**BASE ADDRESS**
DOWN	DOWN	0x220
DOWN	UP	0x230
UP	DOWN	0x240
UP	UP	0x250

The configuration addresses are determined by CPLD U5 and can be changed if needed. Configuration I/O uses 2 contiguous I/O locations starting at the base address. Configuration I/O can be disabled by the FPGA once loaded, to reclaim the I/O space. The configuration jumper settings are readable by the FPGA, allowing the FPGAs internal register decode to follow the configuration address if desired.

CONNECTOR POWER

The power connection on the I/O connectors can supply either 3.3V or 5V power. Supplied power should be limited to 400 mA total. W2 selects the power supplied to P5 and W3 selects the power supplied to P3. When W2 or W3 are in the up position, 5V power is supplied to the connector and associated pull-up resistors. When W2 or W3 are in the down position, 3.3V is supplied.

RS-422 TERMINATION

The 4I38s RS-422 port can be terminated with a 130 Ohm resistor if desired. When W1 Is in the up position, termination is enabled. When W1 is in the down position, termination is disabled.

HARDWARE CONFIGURATION

CONFIGURATION MODE

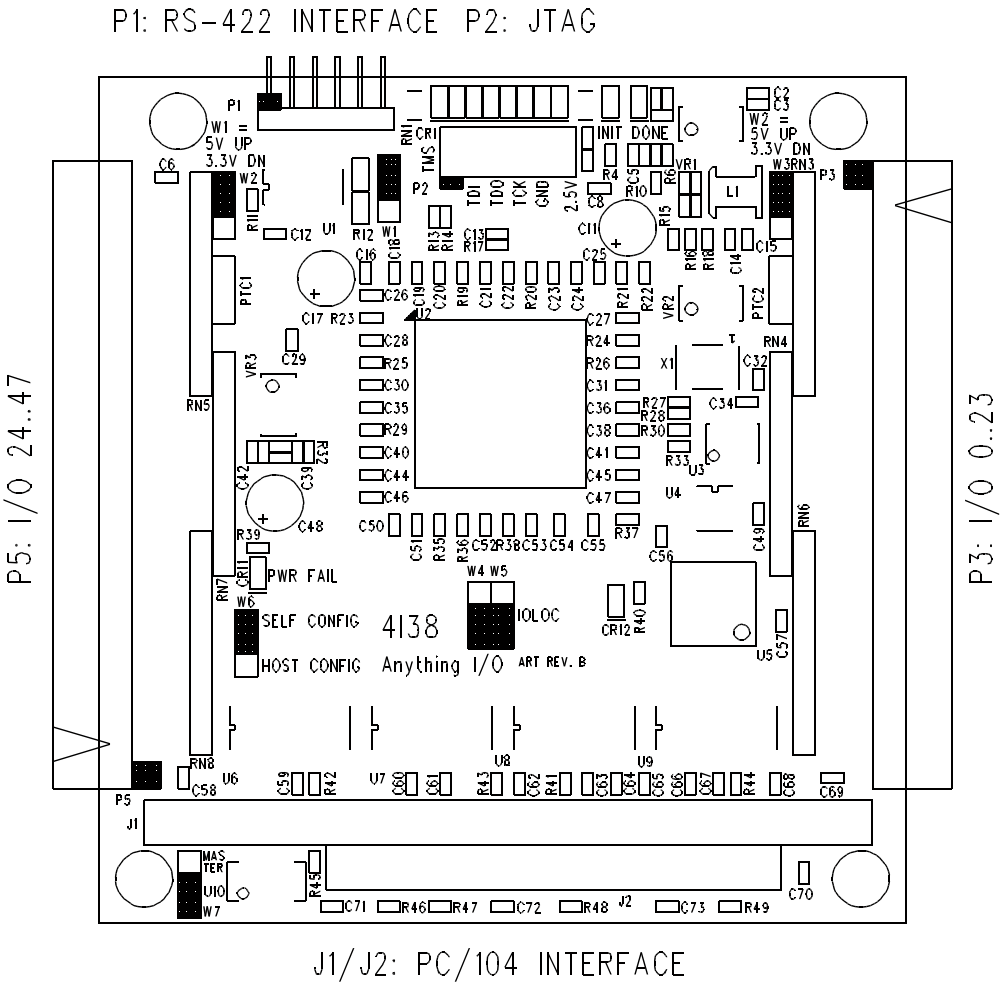
The 4I38s FPGA can be configured via the PC/104 bus or an on card serial EEPROM. W6 determines the configuration mode. When W6 is in the up position (self config), The 4I38 will be configured via the on card serial EEPROM at power up. When W6 is in the down position, The 4I38 must be configured by downloading the configuration file via the PC/104 bus.

MASTER MODE PULL-UPS

The 4I38 can function as a PC/104 bus master (CPU replacement). PC/104 bus masters have strong pull-ups on several open drain signals. These pull-ups are not needed or desired if not running in master mode. W7 determines if these signals are pulled up. When W7 is in the up position, 300 Ohm pull-ups are enabled on /OWS, /MEMCS16, /IOCS16, /REFRESH and /MASTER. When W7 is in the down position, these pullups are disabled. Unless you are using the 4I38 as a CPU replacement, W7 should be left in the down position.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

JTAG CONNECTOR

P2 is a JTAG programming connector. It is not normally used since the 4I38 can be programmed via the PC/104 interface, but can be useful when debugging. Note that this is a **2.5V *JTAG interface, higher voltages may damage the FPGA!***

P2 CONNECTOR PINOUT

PIN	FUNC	
1	TCK	
2	TDI	
3	TDO	
4	TMS	
5	GND	
6	+2.5V	!

RS-422 INTERFACE CONNECTOR

P1 is a RS-422 interface connector that connects to the FPGA. P1 pin-out is as follows:

PIN	FUNC	
1	GND	
2	RX+	NON_INVERTED RECEIVE DATA
3	RX-	INVERTED RECEIVE DATA
4	TX-	INVERTED TRANSMIT DATA
5	TX+	NON_INVERTED TRANSMIT DATA
6	GND	

CONNECTORS

I/O CONNECTORS

P3 and P5 are the 4I38s I/O connectors. These are 50 pin box headers that mate with standard 50 conductor female IDC connectors. For information on which I/O pin connects to which FPGA pin, please see the 4I38IO.PIN file in the 4I38 distribution software package. 4I38M IO connector pinouts are as follows:

P3 CONNECTOR PIN-OUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO0	2	GND	3	IO1	4	GND
5	IO2	6	GND	7	IO3	8	GND
9	IO4	10	GND	11	IO5	12	GND
13	IO6	14	GND	15	IO7	16	GND
17	IO8	18	GND	19	IO9	20	GND
21	IO10	22	GND	23	IO11	24	GND
25	IO12	26	GND	27	IO13	28	GND
29	IO14	30	GND	31	IO15	32	GND
33	IO16	34	GND	35	IO17	36	GND
37	IO18	38	GND	39	IO19	40	GND
41	IO20	42	GND	43	IO21	44	GND
45	IO22	46	GND	47	IO23	48	GND
49	POWER	50	GND				

CONNECTORS

4I38 I/O CONNECTORS

P5 CONNECTOR PIN-OUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO24	2	GND	3	IO25	4	GND
5	IO26	6	GND	7	IO27	8	GND
9	IO28	10	GND	11	IO29	12	GND
13	IO30	14	GND	15	IO31	16	GND
17	IO32	18	GND	19	IO33	20	GND
21	IO34	22	GND	23	IO35	24	GND
25	IO36	26	GND	27	IO37	28	GND
29	IO38	30	GND	31	IO39	32	GND
33	IO40	34	GND	35	IO41	36	GND
37	IO42	38	GND	39	IO43	40	GND
41	IO44	42	GND	43	IO45	44	GND
45	IO46	46	GND	47	IO47	48	GND
49	POWER	50	GND				

PC/104 CONNECTIONS

The 4I38 implements complete connections for the PC/104 interface including full 16 bit I/O and memory interface, all available interrupts, and all DMA channels. The interface can run as a bus master (CPU replacement) For information on which FPGA pin connects to which PC/104 pin, please see the 4I38104.PIN file in the software support package. Note that the .UCF files included with the example configurations can be used as starting points for customer implemented designs.

4I38 OPERATION

FPGA

The 4I38 use a Xilinx Spartan-III FPGA in a 320 pin BGA package The 4I38-1 uses the 1M gate part. The 4I38-1.5 uses the 1.5M gate part.

CONFIGURATION

Before the 4I38 can do anything useful its FPGA must be configured. This can be done by writing a series of bytes from the configuration file to the 4I38 card's configuration data register. (host configuration mode) or by using the serial EEPROM (self configuration mode).

HOST CONFIGURATION MODE

In host configuration mode, before configuration data can be sent to the 4I38 some control register bits must be set up. This is done in the control and status register.

CONFIGURATION REGISTERS

BASE ADDRESS CONFIGURATION DATA REGISTER

BIT	D7	D6	D5	D4	D3	D2	D1	D0
READ	CFGD7	CFGD6	CFGD5	CFGD4	CFGD3	CFGD2	CFGD1	CFGD0
WRITE	CFGD7	CFGD6	CFGD5	CFGD4	CFGD3	CFGD2	CFGD1	CFGD0

BASE ADDRESS+1 CONFIGURATION STATUS & CONTROL REGISTER

BIT	D7	D6	D5	D4	D3	D2	D1	D0
READ	XX	XX	XX	XX	XX	XX	XX	DONE
WRITE	XX	XX	XX	XX	XX	XX	/PROG	/LED

SC4I38

A DOS executable SC4I38.EXE is provided to send files to the 4I38. The source for this program is available on the distribution disk, and can be used as an example for writing a custom version of download software.

OPERATION

SC4I38

SC4I38 is invoked with the FPGA configuration file and the 4I38 configuration base address on the command line:

```
SC4I38 FPGAFILE.BIN 220
```

would send the configuration file FPGAFILE.BIN to the 4I38 with a base address of 0x220. SC4I38 uses binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC4I38 utility sends PROM files directly to the 4I38. BIT files have their headers stripped and are bit reversed before being sent to the 4I38.

CONFIGURATION DISABLE

4I38 cards can disable the configuration hardware after the FPGA chip has been configured. This is useful to reclaim I/O space used by the configuration hardware. It allows, for example, the final I/O address of a FPGA peripheral to be located at the same place as the configuration address. Several of the example configurations do this. Configuration disable is accomplished by driving the DIS pin on the FPGA high. See the 4I38104.PIN file for FPGA pin location of the DIS signal. To disable the configuration hardware once the FPGA is configured, simply assign the DIS pin a high level in the FPGA source file. The DIS pin will then be driven high once the FPGA is configured.

The disadvantage of using configuration disable is that you cannot re-configure the FPGA without reseting the host CPU. (Unless you implement the DIS pin as a host controlled bit)

CONFIGURATION FILE STARTUP OPTIONS

Important: *Because the 4I38s CPLD stops configuration when DONE is asserted, the configuration file startup options must be set so that asserting DONE is the last configuration step.* Suggested startup options are as follows:

FPGA STARTUP CLOCK: **CCLK**

DONE: **6**

ENABLE OUTPUTS: **5**

RELEASE WRITE ENABLE: **4**

RELEASE DLL: **NO WAIT**

OPERATION

EEPROM CONFIGURATION MODE

For bus master master applications and when it is not desired to have to preconfigure the FPGA via the host interface at power up, the 4I38 can be configured via its serial EEPROM. This feature is enabled by setting the configuration mode jumper to "SELF CONFIG". Of course the Serial EEPROM must first be programmed with the desired configuration file.

All access the serial EEPROM is via the FPGA, so programming the serial EEPROM is a "bootstrap" process, where the first step is programming the FPGA with a configuration giving the host access to the serial EEPROM through the FPGA. The IOPR12 configuration has the required SPI interface hardware, so it must be loaded first to be able to we-write the serial EEPROM.

The SCM4I38 program is an example program for writing the serial EEPROM via the PC/104 bus, SCM4I38 programs relys on the IOPR12 configuration file being preloaded into the FPGA before writing the serial EEPROM, as the serial EEPROM can only be accessed through the FPGA.

EXTRA EEPROM SPACE

The serial configuration EEPROM on the 4I38 has a capacity of 512K bytes (4I38-1) or 1.M bytes (4I38-1.5), but the configuration bit file for the 1M Spartan 3 chip is only ~405K bytes, leaving ~106 K bytes free for FPGA accessible non volatile storage. The 1.5M gate Spartan 3 chip uses only 652K byte of the serial EEPROM leaving ~370K bytes free. This storage can be used for non-volatile settings or program storage in stand-alone 4I38 applications.

CLOCK SIGNALS

Seven of the 8 available clock signals are used by the 4I38, three for PC/104 bus and system clock and 4 available on the I/O lines:

GCLK0	/SMEMWR	GCLK1	UNUSED
GCLK2	/IOWR	GCLK3	50 MHZ CLOCK
GCLK4	I/O 1	GCLK5	I/O 0
GCLK6	I/O 25	GCLK7	I/O 24

OPERATION

LEDS

The 4I38 has 8 status LEDS, . These LEDS can be used for any purpose, and can be helpful as a simple debugging feature. A low output signal from the FPGA lights the LED. See the 4I38104.PIN file for FPGA pin locations of the LED signals.

IO LEVELS

The FPGA used on the 4I38 is a Spartan3. The Spartan3 supports many I/O standards. The 4I38 does not support use of the I/O standards that require input reference voltages, also VCCIO on the banks that connect to P3 and P5 are fixed at 3.3V so only 5 I/O options can be used on P1 and P2. The available I/O options for P3 and P25are are LVTTL, LVCMOS_33, LVDCI_33, and LVDCI_33_DV2 .

Note that the Spartan3 chip is _NOT_ 5V tolerant and should not have signals exceeding 3.3V applied to its inputs.

TERMINATION

The FPGAs used on the 4I38 support series and parallel termination that can be programmed on a pin-for-pin basis. This feature is called DCI. The 4I68 supports DCI on all I/O pins. The DCI reference resistors are all 100 Ohm 1%.

POWER SUPPLY

The 4I38 uses on card regulators to supply the 3.3VCC, 2.5VAUX/VIO and 1.2VCORE core power for the FPGA. The core power supply is rated at 2.5 Amp. The 3.3V and 2.5V power are limited to 600 mA. All power supplies are sourced from the 5V bus power.

SUPPLIED CONFIGURATIONS

IOPR12

The IOPR12 configuration creates a simple 48 bit (4I38) parallel I/O port. The port base address follows the configuration address 16 IO locations are used. The IOPR12 configuration is a word device, all accesses read or write 16 bit words. Each I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. For information on the register map of the IOPR12 configuration, see the regmap file in the /configs/IOPR12 directory of the 4I38 distribution disk. IOPR12 asserts DIS to disable the configuration hardware once the FPGA is configured, so the 4I38 will have to be reset to allow re-configuration. IOPR12 also contains a simple SPI interface to allow programming of the configuration serial EEPROM.

REFERENCE INFORMATION

SPECIFICATIONS

	MIN	MAX	NOTES
SUPPLY VOLTAGE	4.5V	5.25V	
SUPPLY CURRENT	100	1000 mA	Depends on FPGA configuration
3.3V CURRENT SUPPLIED TO P3,P5	----	400 mA	.
5V CURRENT SUPPLIED TO P3,P5	----	400 mA	
1.2V CORE POWER CURRENT	----	2.5A	
TEMPERATURE -C VERSION	0^{o}C	70^{o}C	
TEMPERATURE -I VERSION	-40^{o}C	85^{o}C	