4I39
RS-422 ANYTHING I/O
MANUAL

V1.0

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GENERAL

DESCRIPTION

The MESA 4I39 is a communication oriented programmable I/O card for the PC/104 bus. The 4I39 has 8 full duplex RS-422 /485 interfaces that are isolated from PC/104 ground and 24 general purpose TTL I/O pins. The 4I39 uses a 200K gate Spartan2 FPGA. The FPGA is downloadable from the PC/104 bus side, allowing creation of almost any kind of specialized I/O function, even including micro-controllers in the FPGA.

Several pre-made functions are provided, including a simple loopback function, 8 channel UART, SSI absolute encoder interface and others. VHDL source is provided for all examples.

The differential interfaces can be use in full duplex (RS-422) or half duplex (RS-485) modes. Differential I/O is galvanically isolated from system ground.

All TTL I/O bits are 5V tolerant and can sink 24 mA. Pullup resistors are provided for all pins so that they may be connected directly to opto-isolators, contacts etc.

4I39 TTL I/O uses a 50 pin connector with I/O module rack compatible pinouts and interleaved grounds, compatible with Mesa's 'Anything I/O ' daughter cards.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 4I39 card is oriented in an upright position, that is, with the PC/104 connectors towards the person doing the configuration.

CONFIGURATION I/O DECODE

The FPGA chip that is the heart of the 4I39 is based on static RAM technology. This means that at power up or after a reset the FPGA is empty and must be configured to do whatever specific task is required of it. This configuration information is sent to the over the PC/104 bus as a sequence of bytes. The I/O location where these bytes are sent is selected by 2 jumpers on the 4I39 card, W3 and W4. The following table shows the standard I/O addresses:

W3	**W4**	**BASE ADDRESS**
DOWN	DOWN	0x220
DOWN	UP	0x230
UP	DOWN	0x240
UP	UP	0x250

The configuration addresses are determined by CPLD U12 and can be changed if needed. Configuration I/O uses 2 contiguous I/O locations starting at the base address. Configuration I/O can be disabled by the FPGA once loaded, to reclaim the I/O space.

PULLUP ENABLE

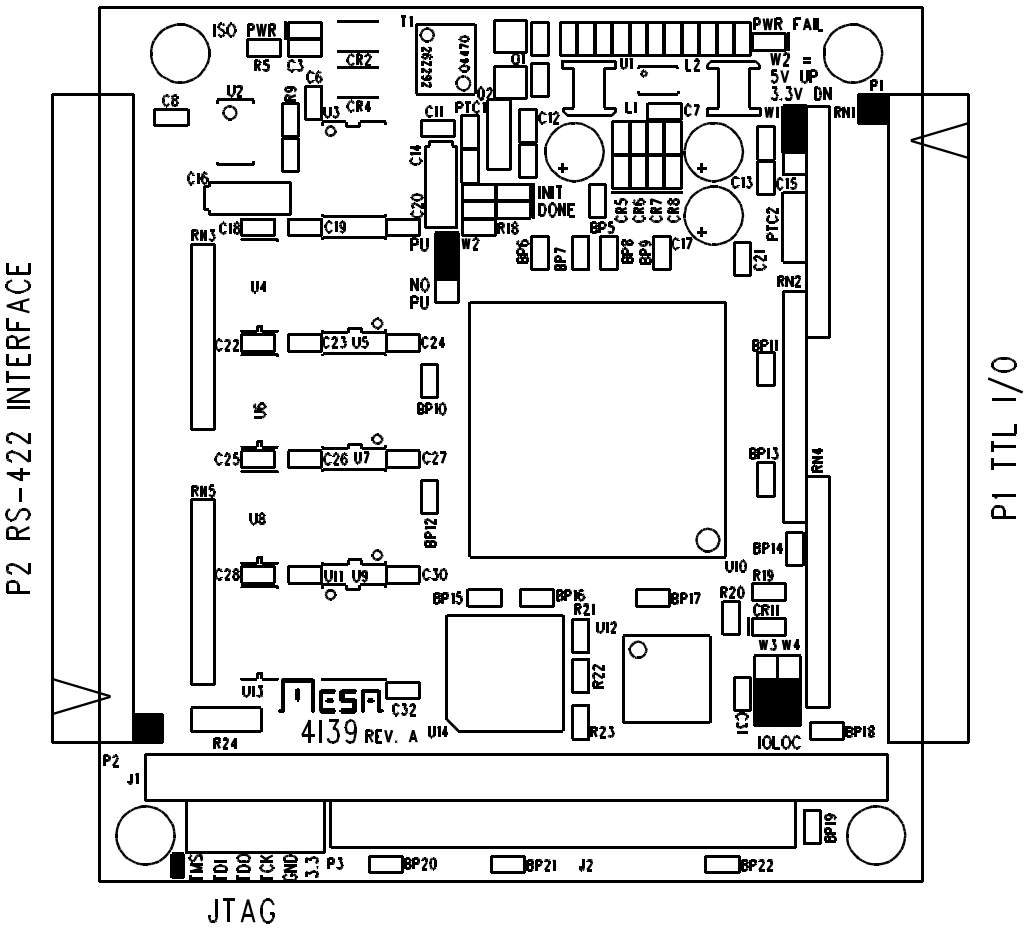
The Xilinx FPGA on the 4I39 has the option of having weak pullups on all I/O pins at powerup or reset. This may be desirable if the 4I39 is used without its 3.3K pullups on I/O pins. To enable the built-in pullups, jumper W2 should be placed in the UP position. To disable the internal pullups (the default setting), W3 should be in the dOWN position.

TTL CONNECTOR POWER

The power connection on P1 can supply either 3.3V or 5V power. Supplied power should be limited to 400 mA total. W1 select s the power supplied to P1. When W1 is in the up position, 5V power is supplied to the connector and associated pullup resistors. When W1 is in the down position, 3.3V is supplied.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

4I39 JTAG CONNECTOR

P3 is a JTAG programming connector. It is not normally used since the 4I39 can be programmed via the PC/104 interface, but can be useful when debugging. The JTAG chain includes the on card CPLD, So if you are using JTAG you must set the XC9536XL CPLD to ‘BYPASS".

P3 CONNECTOR PINOUT

PIN	FUNC
1	TCK
2	TDI
3	TDO
4	TMS
5	GND
6	+3.3V

CONNECTORS

I/O CONNECTORS

P1 and P2 are the 4I39s I/O connectors. P1 is the TTL I/O connector and P2 is the Isolated RS-422 connector. Both are 50 pin shrouded headers that mate with standard 50 conductor female IDC connectors. For information on which I/O pin connects to which FPGA pin, please see the 4I39IO.PIN file on the 4I39 distribution disk. 4I39 IO connector pinouts are as follows:

P1 CONNECTOR PINOUT: TTL I/O

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO0	2	GND	3	IO1	4	GND
5	IO2	6	GND	7	IO3	8	GND
9	IO4	10	GND	11	IO5	12	GND
13	IO6	14	GND	15	IO7	16	GND
17	IO8	18	GND	19	IO9	20	GND
21	IO10	22	GND	23	IO11	24	GND
25	IO12	26	GND	27	IO13	28	GND
29	IO14	30	GND	31	IO15	32	GND
33	IO16	34	GND	35	IO17	36	GND
37	IO18	38	GND	39	IO19	40	GND
41	IO20	42	GND	43	IO21	44	GND
45	IO22	46	GND	47	IO23	48	GND
49	POWER	50	GND				

CONNECTORS

4I39 I/O CONNECTORS

P2 CONNECTOR PINOUT: RS-422 I/O

PIN	FUNC	PIN	FUNC	PIN	FUNC
1	/IN0	2	IN0	3	IGND
4	/OUT0	5	OUT0	6	IGND
7	/IN1	8	IN1	9	IGND
10	/OUT1	11	OUT1	12	IGND
13	/IN2	14	IN2	15	IGND
16	/OUT2	17	OUT2	18	IGND
19	/IN3	20	IN3	21	IGND
22	/OUT3	23	OUT3	24	IGND
25	/IN4	26	IN4	27	IGND
28	/OUT4	29	OUT4	30	IGND
31	/IN5	32	IN5	33	IGND
34	/OUT5	35	OUT5	36	IGND
37	/IN6	38	IN6	39	IGND
40	/OUT6	41	OUT6	42	IGND
43	/IN7	44	IN7	45	IGND
46	/OUT7	47	OUT7	48	IGND
49	KEY	50	IGND		

RS-422 polarities are such that the INX and OUT X pins are the same polarity as the FPGA pins, while the /INX and /OUTX pins are inverted.

CONNECTORS

PC/104 CONNECTIONS

The 4I39 implements connections for fairly complete PC/104 interface including full 16 bit I/O and memory interface, all available interrupts, and all DMA channels. For information on which FPGA pin connects to which PC/104 pin, please see the 4I39P104.PIN file on the distribution disk. Note that the .UCF files included with the example configurations can be used as starting points for customer implemented designs.

4I39 OPERATION

FPGA

The 4I39 use a 200 K gate Xilinx Spartan-II FPGA in a 208 pin QFP package, the XC2S200-PQ208.

CONFIGURATION

Before the 4I39/4I39M can do anything useful it must have its FPGA configuration data downloaded from the host CPU to the FPGA on the 4I39. This is done by writing a series of bytes from the configuration file to the 4I39 card's configuration data register. Before that data can be sent some control register bits must be set up. This is done in the control and status register.

CONFIGURATION REGISTERS

BASE ADDRESS CONFIGURATION DATA REGISTER

BIT	D7	D6	D5	D4	D3	D2	D1	D0
READ	CFGD7	CFGD6	CFGD5	CFGD4	CFGD3	CFGD2	CFGD1	CFGD0
WRITE	CFGD7	CFGD6	CFGD5	CFGD4	CFGD3	CFGD2	CFGD1	CFGD0

BASE ADDRESS+1 CONFIGURATION STATUS & CONTROL REGISTER

BIT	D7	D6	D5	D4	D3	D2	D1	D0
READ	XX	XX	XX	XX	XX	XX	XX	DONE
WRITE	XX	XX	XX	XX	LED	/WRITE	/PROG	/CS

SC4I39

A DOS executable SC4I39.EXE is provided to send configuration files to the 4I39. The Pascal and C source for this program is available on the distribution disk, and can be used as an example for writing a custom version of download software. SC4I39 is invoked with the FPGA configuration file and the 4I39 configuration base address on the command line:

```
SC4I39 FPGAFILE.BIN 220
```

would send the configuration file FPGAFILE.BIN to the 4I39 with a base address of 220 hex.

OPERATION

SC4I39

SC4I39 uses binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC4I39 utility sends PROM files directly to the 4I39. BIT files have their headers stripped and are bit reversed before being sent to the 4I39.

CONFIGURATION DISABLE

4I39 cards can disable the configuration hardware after the FPGA chip has been configured. This is useful to reclaim I/O space used by the configuration hardware. It allows, for example, the final I/O address of a FPGA peripheral to be located at the same place as the configuration address. Several of the example configurations do this. Configuration disable is accomplished by driving the DIS pin on the FPGA high. See the 4I39P104.PIN file for FPGA pin location of the DIS signal. To disable the configuration hardware once the FPGA is configured, simply assign the DIS pin a high level in the FPGA source file. The DIS pin will then be driven high once the FPGA is configured.

The disadvantage of using configuration disable is that you cannot re-configure the FPGA without reseting the host CPU. (Unless you implement the DIS pin as a host controlled bit)

OPERATION

CLOCK SIGNALS

The 4 FPGA clock signals on the 4I39 are routed to 4 separate clock sources. GCLK0 connects to a 48 MHz crystal oscillator on the 4I39 card, GCLK1 connects to the PC/104 /IOW signal, GCLK2 connects to the IO0 connector pin, and GCLK3 connects to the PC/104 SYSCLK signal.

LEDS

The 4I39 has 9 status LEDS. 5 are dedicated and 4 are driven by free FPGA pins and can be used as general purpose status indicators.

LED	COLOR	FUNCTION
CR1	GREEN	ISOLATED POWER ON INDICATOR
CR3	RED	FPGA POWER FAIL
CR5	GREEN	GENERAL PURPOSE STATUS
CR6	GREEN	GENERAL PURPOSE STATUS
CR7	GREEN	GENERAL PURPOSE STATUS
CR8	GREEN	GENERAL PURPOSE STATUS
CR9	RED	/INIT -- LIT IF INIT IS LOW
CR10	RED	DONE -- LIT IF DONE IS LOW
CR11	YELLOW	CPLD CONFIG I/O BIT

When the FPGA is configured properly, all red LEDs should be extinguished, and CR1 (Isolated power) should be illuminated. The general purpose status LEDs have their anodes connected to 3.3V power through resistors, so a ‘LOW’ level FPGA output illuminates the LED.

OPERATION

ISOLATED POWER SUPPLY DRIVE

The on card power supply for the isolated RS-422 interface gets its drive signals from the FPGA. Two push-pull non-overlapping drive signals are required, PSDRIVE(0) and PSDRIVE(1). The optimum frequency is ~400 KHz. The following snippet of VHDL code illustrates one way to generate the required signals:

```
signal PC: std_logic_vector(6 downto 0);

GateDrive : process(SynClk)        -- this is for the on card isolated power supply

begin

-- DC-DC converter gate drive

-- 48 MHz /128 = 375 KHz

-- 15/16 drive duty cycle for ~160 ns of non-overlap

        if SynClk'event and SynClk = '1' then

                PC <= PC +1;

        end if;

        PSDRIVE(0) <= (      PC(6)) and (PC(5) or PC(4) or PC(3));

        PSDRIVE(1) <= (not PC(6)) and (PC(5) or PC(4) or PC(3));

end process;
```

OPERATION

RS-422 ENABLES

The 4I39 can enable and disable (float) its RS-422 drivers in pairs. There are four ENABLE signals, one for each driver pair. For full duplex applications these enables can simply be tied high in the FPGA. For half duplex protocols the ENABLE signals can be controlled by the transmitter logic. Because the driver chips are enabled in pairs, a half duplex link uses two RS-422 channels. That is if ENA0 is used to control the OUT0 pair, the OUT1 pair also gets enabled and disabled at the same time, making it useless for most applications.

ENA0 Enables driver for OUT0 and OUT1

ENA1 Enables driver for OUT2 and OUT3

ENA2 Enables driver for OUT4 and OUT5

ENA3 Enables driver for OUT6 and OUT7

RS-422 TERMINATION

The RS-422 inputs of the 4I39 are terminated via socketed resistor networks RN3 and RN5. These are 100 Ohm 8 pin 4 resistor SIP networks. These resistor networks may be removed for multi drop applications where the 4I39 is in not at the end of the RS422/RS-485 line. RN5 terminates IN0 through IN3 and RN3 terminates IN4 through IN7.

TTL IO LEVELS

The Xilinx FPGAs used on the 4I39 have programmable I/O levels for interfacing with different logic families. The 4I39 does not support use of the I/O standards that require input reference voltages, so only 5 I/O options can be used. The available I/O options are LVTTL (5V tolerant), PCI33_5 (5V tolerant), PCI33_3, PCI66_3, and LVCMOS2. Two of the I/O options allow 5V inputs. You must make sure to use 5V compatible IO options on the PC/104 part of your designs, because the PC/104 bus uses 5V levels. I/O levels of the users I/O pins do not have to be +5V compatible if not needed, but it is suggested to use one of the 5V tolerant I/O standards to avoid possible damage if larger than 3.3V signals are applied to I/O pins.

Note that even though the 4I39s FPGA can tolerate 5V signal inputs, its outputs will not swing to 5V. The outputs are push pull CMOS outputs that will drive to the output supply rail of 3.3V. This is sufficient for TTL compatibility but may cause problems with some types of loads. For example when driving an LED that has its anode connected to 5V, the 3.3V high level may not completely turn the LED off. To avoid this problem, either drive loads that are ground referred, Use 3.3V as the VCC for VCC referred loads, or tristate the output signals when no drive is desired (open drain).

SUPPLIED CONFIGURATIONS

I39LOOP

The I39LOOPconfiguration creates a simple loopback configuration to test the RS-422 and TTL I/O. The eight RS-422 output bits and the four enable bits can be controlled via writes to registers and the eight RS422 inputs can be polled. The TTL port is accessed as two 12 bit ports. Each TTL I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. For information on the register map of the I39LOOP configuration, see the regmap file in the /configs/I39LOOP directory of the 4I39 distribution disk.

I39SSI

The I39SSI configuration is an interface to eight SSI type absolute encoders. It supports data lengths from 1 to 32 bits, clock rates from <1 KHz to 10 MHz, FIFOed data path, and an automatic timed acquisition of all channels via a built in sample rate generator. The I39SSI configuration can also generate an interrupt when data is available. For information on the register map of the I39SSI configuration, see the regmap file in the /configs/I39SSI directory of the 4I39 distribution disk.

REFERENCE

SPECIFICATIONS

POWER	**MIN**	**MAX**	**NOTES**:
POWER SUPPLY	4.5V	5.5V	+- 10%
POWER CONSUMPTION:	----	500 mA	Configuration dependent
DATA RATE (RS-422)	10 MHz	----	
RS-422 ISOLATION VOLTAGE	500VDC	----	1M 1/W antistatic resistor from isolated gnd to system gnd
TTL I/O PORT SOURCE CURRENT	-24 mA	----	2.4 VOH
TTL I/O PORT SINK CURRENT	24 mA	----	0.4 VOL
TTL I/O PORT PULLUP RESISTORS	3.3K	3.3K	Removeable
RS-422 TERMINATION	100 Ohm	100 Ohm	Removeable
RS-422 COMMON MODE RANGE	-7V	+12V	Relative to isolated ground
RS-422 ESD RATING	10KV	---	Human body model