5I21
SERIAL ANYTHING I/O MANUAL

1.2

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GENERAL

DESCRIPTION

The MESA 5I21 is a programmable serial interface card for the PCI bus. The 5I21 is designed for applications using RS-422 and RS-485 interfaces. The 5I21 can support up to 12[1] full duplex RS-422 or half duplex RS-485 serial links with baud rates up to 10 M baud[2] The 5I21 uses a 400K gate Spartan3 FPGA and a bus mastering PCI bridge for high performance.

Since all serial logic is FPGA based, almost any RS-422/RS485 protocol can be supported. The I/O connector is a 68 pin high density type compatible with standard 100 ohm differential cables. On card serial line termination includes idle line pullups and pulldowns to guarantee a valid undriven input state.

The 5I21 is suitable for high performance motion control systems, Industrial I/O, Custom real time distributed I/O, time code generation, supporting legacy hardware, and almost any high speed serial interface application that requires a flexible, high performance, universal RS422/485 serial interface card.

Notes:

1. Higher bit rates are possible with different differential driver/receiver chips, contact MESA

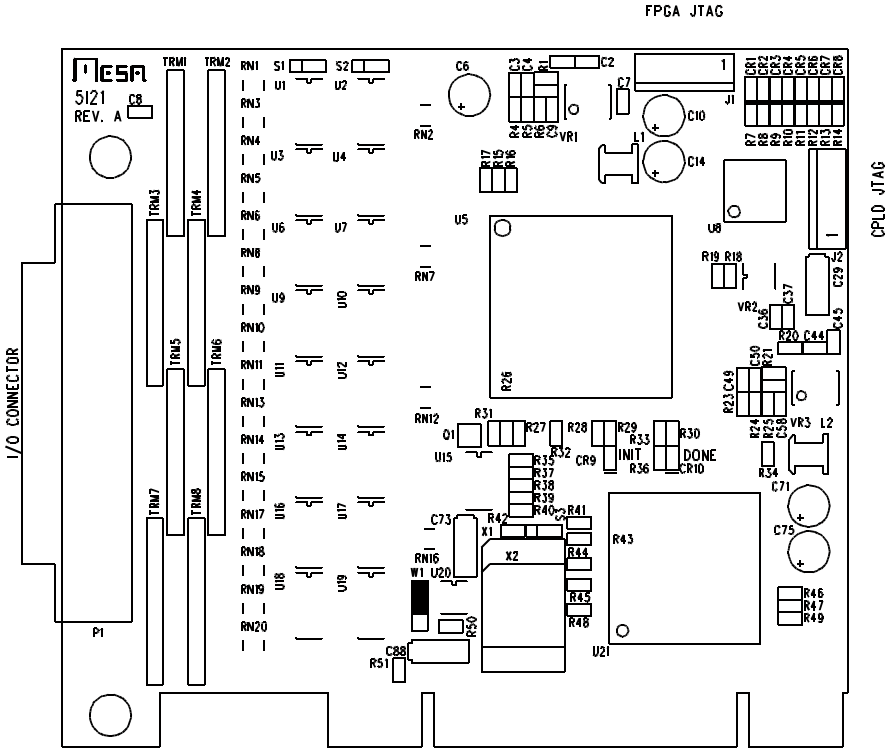
2. A 16 channel version is available, contact MESA.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 5I21 card is oriented in an upright position, that is, with the PCI connector on the bottom and the white PCB markings right side up.

CONNECTOR LOCATIONS AND DEFAULT W1 POSITION



HARDWARE CONFIGURATION

EEPROM ENABLE

The PLX9054 PCI-Local bus bridge chip is configured at power up via a serial EEPROM. If the EEPROM is somehow mis-programmed or corrupted, it can be impossible to re-write the EEPROM from the PCI bus. To avoid this problem, The EEPROM can be temporarily disabled. W1 controls the EEPROM enable function, When W1 is in the up position (default) the EEPROM is enabled. When W1 is in the down position, the EEPROM is disabled. To fix a broken EEPROM setup, you must power up the 5I21 card with the EEPROM disabled, Enable the EEPROM, and re-write the EEPROM.

CONNECTORS

SERIAL I/O CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	CH0+	35	CH0-	2	CH1+	36	CH1-
3	CH2+	37	CH2-	4	CH3+	38	CH3-
5	CH4+	39	CH4-	6	CH5+	40	CH5-
7	CH6+	41	CH6-	8	CH7+	42	CH7-
9	CH8+	43	CH8-	10	CH9+	44	CH9-
11	CH10+	45	CH10-	12	CH11+	46	CH11-
13	CH12+	47	CH12-	14	CH13+	48	CH13-
15	CH14+	49	CH14-	16	CH15+	50	CH15-
17	CH16+	51	CH16-	18	CH17+	52	CH17-
19	CH18+	53	CH18-	20	CH19+	54	CH19-
21	CH20+	55	CH20-	22	CH21+	56	CH21-
23	CH22+	57	CH22-	24	CH23+	58	CH23-
25	GND	59	GND	26	GND	60	GND
27	GND	61	GND	28	GND	62	GND
29	GND	63	GND	30	GND	64	GND
31	GND	65	GND	32	GND	66	GND
33	+5V	67	GND	34	+5V	68	GND

CONNECTORS

FPGA JTAG CONNECTOR PINOUT

J1 is the JTAG connector for the FPGA J1 pinout is as follows:

PIN	FUNCTION	DIRECTION
1	TMS	TO FPGA
2	TDI	TO FPGA
3	TDO	FROM FPGA
4	TCK	TO FPGA
5	GND	XX
6	2.5V	

CPLD JTAG CONNECTOR PINOUT

J2 is the JTAG connector for the CPLD. J2 pinout is as follows:

PIN	FUNCTION	DIRECTION
1	TMS	TO CPLD
2	TDI	TO CPLD
3	TDO	FROM CPLD
4	TCK	TO CPLD
5	GND	XX
6	3.3V	XX

OPERATION

FPGA

The 5I21 use a Xilinx Spartan-III 400K gate FPGA in a 208 pin QFP package: XC3S400-PG208.

FPGA PINOUT

The local bus and I/O interface FPGA pinouts are described in the 5I21INFC.PIN and 5I21IO.PIN files in CONFIGS directory of the distribution disk. The 5I21IO.PIN file may be used as a template for custom configurations.

MEMORY AND I/O REGIONS

The PLX9054 PCI bridge local configuration registers can be accessed via I/O or memory. These are used to setup the PCI bridge, and for manipulating the I/O bits when configuring the FPGA.

BAR	MEM - I/O	WIDTH	RANGE
BAR 0	I/O	32 BITS	128 BYTES
BAR 1	MEMORY	32 BITS	128 BYTES

The PLX9054 PCI bridge allows for 2 separate memory and I/O regions to be mapped to the local bus that connects to the FPGA. The default EEPROM configuration sets these up as follows:

BAR	ADDRESS SPACE	MEM - I/O	WIDTH	RANGE
BAR 2	0	I/O	32 BITS	256 BYTES
BAR 3	1	MEMORY	32 BITS	64K BYTES

LOCAL BUS INTERFACE

The 5I21 uses the multiplexed local bus option of the PLX9054 bridge chip to save FPGA pins. All FPGA interface logic latch the LAD bus when ADS is active to create an internal address

OPERATION

CONFIGURATION

Before the 5I21 can do anything useful it must have its FPGA configuration data downloaded from the host CPU to the FPGA on the 5I21. This is done by writing a series of bytes from the configuration file to the 5I21 card's configuration data register. Configuration data is written a byte at a time (Right justified) to any of the I/O or memory bus space regions mapped to the 5I21s local bus.

The FPGA configuration control bits must be manipulated before configuration data can be sent to the FPGA. These control bits are controlled via GPIO pins of the PLX9054 PCI bridge. The PLX9054s GPIO pins are connected to the following FPGA configuration pins:

GPIO	DIRECTION	FPGA	ALTERNATE
GPI	IN	DONE	/DACK
GPO	IN	/PROGRAM	/DREQ

Note that the DONE and /PROGRAM bits are multiplexed with DMA control lines. If these DMA control lines are needed, the DISABLECONF pin on the FPGA needs to be asserted or a /DREQ signal will reset the FPGA.

UNUSED PINS

Due to the preferred idle local bus state on the 5I21, unused FPGA pins must be pulled up. This can be set in the 'Generate Programming File" properties box, configuration options tab, Unused IOB selection list.

SC5I21

A DOS utility program SC5I21.EXE is provided to send configuration files to the 5I21. The Pascal and C source for this program is available on the distribution disk, and can be used as an example for writing a custom version of download software. SC5I21 is invoked with the FPGA configuration file and the 5I21 configuration base address on the command line:

```
SC5I21 FPGAFILE.BIN
```

SC5I21 uses binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC5I21 utility sends PROM files directly to the 5I21. BIT files have their headers stripped and are bit reversed before being sent to the 5I21.

OPERATION

CONFIGURATION

SC9054W

Another utility SC9054W is provided for Windows 2000 and Windows XP This utility requires the PLX9054.SYS driver and PLXAPI.DLL API SHIM to work. The source for SC9054W can be used as an example of how to access the configured 5I21cards under Windows 2K or XP.

SC9054W use binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC9054W utility sends PROM files directly to the 5I21. BIT files have their headers stripped and are bit reversed before being sent to the 5I21.

OPERATION

CLOCK SIGNALS

The FPGA has one on card clock source. The on card clock is 48 MHz routed to GCLK3 (FPGA pin 77). This functions as the FPGA system clock and the local bus interface clock.

LEDS

The 5I21 has 8 FPGA driven user LEDs. The user LEDs can be used for any purpose, and can be helpful as a simple debugging feature. A low output signal from the FPGA lights the LED. See the 5I21IO.PIN file for FPGA pin locations of the LED signals.

TERMINATION

The RS-422/485 I/O pairs are terminated on card with plug in resistor networks. These resistor networks each terminate 4 signal pairs. Termination should always be used on receive inputs unless the 5I21 is not at the end of the signal cable. To disable termination, the proper resistor network must be removed. The following table shows which termination resistor networks connect to which I/O signals:

TRM8	CH0,CH2,CH4,CH6	TRM7	CH1,CH3,CH5,CH7
TRM6	CH8,CH10,CH12,CH14	TRM5	CH9,CH11,CH13,CH15
TRM4	CH16,CH18,CH20,CH22	TRM3	CH17,CH19,CH21,CH23

For RS-422 applications where some channels are always used for transmit and some channels are always used for receive, and if the transmit and receive pairs are selected properly, it possible to remove the unneeded termination resistors on the transmit outputs. For example: If we configure the FPGA for 12 RS-422 channels, with all transmits on even channel numbers and all receives on odd channels numbers, we could remove TRM4,TRM6, and TRM8

POWER SUPPLY

The 5I21 uses on card switching regulators to supply the 3.3VCC, 2.5VAUX/VIO and 1.2VCORE core power for the FPGA. The core power supply is rated at 1 Amp. The 3.3V and 2.5V power are limited to 600 mA. All power supplies are sourced from the 5V bus power.

OPERATION

FPGA TO RS-422/485 INTERFACE

The 5I21 supports 12 full duplex RS-422 channels or 12 half duplex RS-485 channels. Due to FPGA and driver chip pin limitations the 24 available data bits on the FPGA are shared between serial data in and serial data out. Serial data out must also be inverted. Separate receive and transmit enables are provided for each pair of interface channels. The transmit and receive enables for a given pair of channels must not be asserted simultaneously. For example:

The first serial data pair:

CH0 DATA

CH2 DATA

are controlled by

CH0_2RXEN and CH0_2TXEN

and the second serial data pair:

CH1 DATA

CH3 DATA

are controlled by

CH1_3RXEN and CH1_3TXEN

So for example in a RS-422 type application with permanently enabled transmit drivers, transmits on CH0 and CH2 and receives on CH1 and CH3:

CH0DATA is an output (inverted RS-422 data)

CH2DATA is an output (inverted RS-422 data)

CH0_2TXEN is set high CH0_2RXEN is set low

CH1 DATA is an input (true RS-422 data)

CH3 DATA is an input (true RS-422 data)

CH1_3TXEN is set low and CH1_3RXEN is set high

OPERATION

FPGA TO RS-422/485 INTERFACE

In a RS-485 type half duplex applications with direction control, transmit and receive on CH0:

During Transmit:

CH0DATA is an output (inverted RS-485 transmit data)

CH2DATA is an output (and not useable)

CH0_2TXEN is set high CH0_2RXEN is set low

During Receive:

CH0DATA is an input (true RS-485 receive data)

CH2DATA is an input (and not useable)

CH0_2TXEN is set low CH0_2RXEN is set high

SUPPLIED CONFIGURATIONS

5I21LOOP

The IOPR24 configuration provides a simple way to check that all the I/O pins are OK and that most of the host interface is working. A loopback program (5I21LOOP) is provided for doing this testing. 5I21LOOP depends on an external loopback cable that connects CH0 to CH1, CH2 to CH3 etc etc. All combinations of inputs and outputs are tested. In addition, a 32 bit register readback test is performed to verify 32 bit local data bus functionality.

REFERENCE

SPECIFICATIONS

POWER	**MIN**	**MAX**	**NOTES**:
POWER SUPPLY	4.5V	5.5V	
POWER CONSUMPTION:	----	700 mA	Depends on FPGA Configuration
MAX 5V CURRENT TO I/O CONNS	---	500 mA	
SERIAL I/O SPECIFICATIONS			
COMMON MODE RANGE	-7V	+12V	
DIFFERENTIAL OUTPUT VOLTAGE	2.0V	—	50 Ohm load
DATA RATE	DC	10 Mbps	
ENVIRONMENTAL			
TEMPERATURE RANGE -C version	0 °C	+70 °C	
TEMPERATURE RANGE -I version	-40 °C	+85 °C	