7I46 MANUAL

6 channel SPI breakout

V1.0

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GENERAL

DESCRIPTION

The 7I46 is a simple passive breakout board designed to connect up to 6 SPI devices to a single 50 pin Anything I/O connector. 10 pin headers are used for the SPI signals. The pinout matches Mesas SPI device pinouts and also supplies 5V power to the SPI device. A high side power switch allows AUX 5V power suppled to the the 7I46 to be routed to the SPI devices, the SPI power will be removed when the Anything I/Os cable power is off, avoiding possible back-powering of the FPGA card from external AUX 5V supply.

The controller connection is a 50 pin header that matches the pinout of Mesa's Anything I/O cards. All RS-422 interface connections use pluggable Phoenix compatible 3.5 mm screw terminals.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I46 card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side.

DEFAULT CONFIGURATION

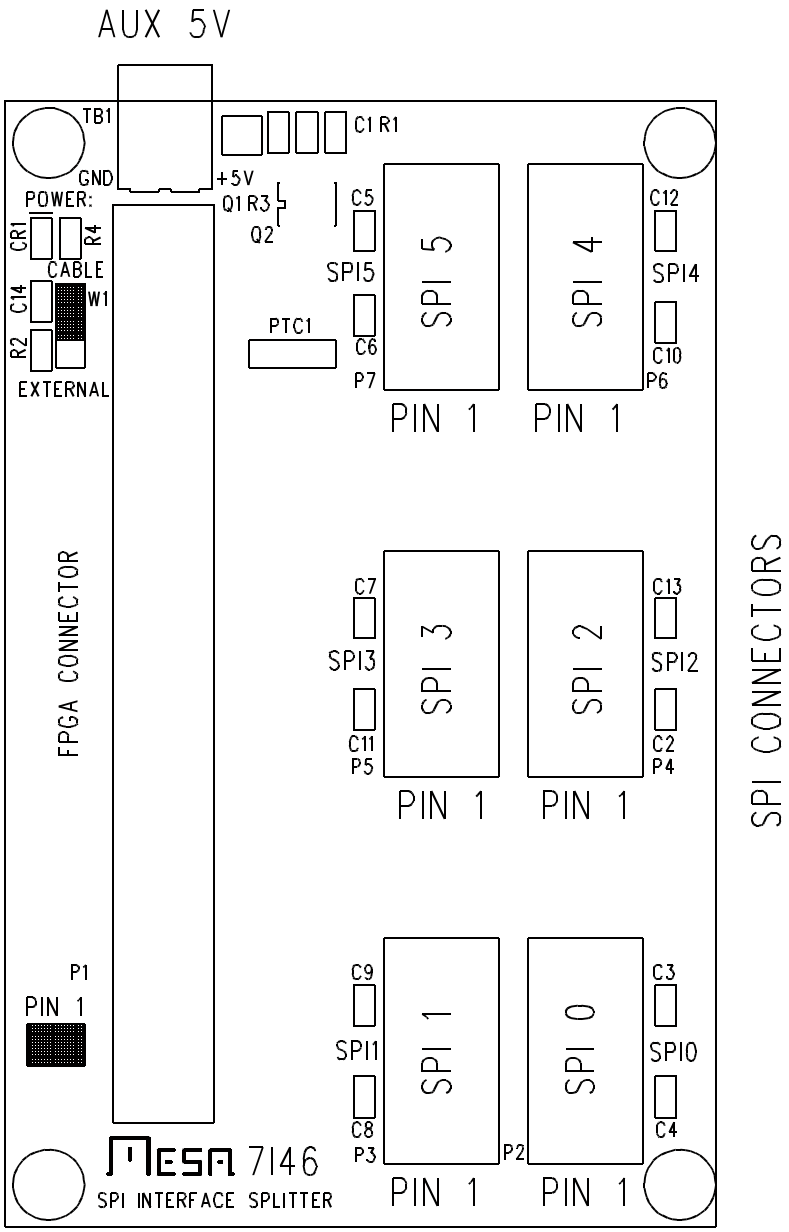
JUMPER	FUNCTION	DEFAULT SETTING
W1	CABLE/AUX 5V POWER	UP = CABLE POWER

CABLE POWER ENABLE

The 7I46 can supply I/O power to P2 through P7 via TB1 or via the 50 conductor flat cable. If W1 is in the"UP" position, flat cable power is used. If W1 is on the "DOWN" position, TB1 power is used.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector J1 connects to the anything I/O card/motion controller. This can be a male 50 pin header on the top of the 7I46 card or a female 50 conductor header on the bottom side of the 7I46 depending on 7I46 model.

PIN	FUNCTION	DIRECTION	PIN	FUNCTION	DIRECTION
1	FRAME0	TO 7I46	25	FRAME3	TO 7I46
3	DOUT0	TO 7I46	27	DOUT3	TO 7I46
5	CLK0	TO 7I46	29	CLK3	TO 7I46
7	DIN0	FROM 7I46	31	DIN3	FROM 7I46
9	FRAME1	TO 7I46	33	FRAME4	TO 7I46
11	DOUT1	TO 7I46	35	DOUT4	TO 7I46
13	CLK1	TO 7I46	37	CLK4	TO 7I46
15	DIN1	FROM 7I46	39	DIN4	FROM 7I46
17	FRAME2	TO 7I46	41	FRAME5	TO 7I46
19	DOUT2	TO 7I46	43	DOUT5	TO 7I46
21	CLK2	TO 7I46	45	CLK5	TO 7I46
23	DIN2	FROM 7I46	47	DIN5	FROM 7I46
			49	+5V PWR	TO 7I46

Note: all even pins are grounded. Signal names shown are for SPI interface on FPGA card. Since the 7I46 is a passive device the 7I46 breakout can be used for other signal types.

AUX 5V POWER

2 pin pluggable terminal TB1 can be used to supply 5V power to the SPI connectors on the7I46. This is suggested for most applications as the SPI devices will typically will draw more current than can be supplied via the FPGA flat cable. TB1 has the following pinout:

PIN	FUNCTION
1	5V
2	GND

CONNECTORS

SPI CONNECTOR PINOUT

The SPI connectors are 10 pin .1" pitch male headers. Suggested mating connector is AMP PN 1658622-1. This is an IDC receptacle for 10 conductor .050 flat cable. SPI signal integrity depends on wiring order, so if flat cable is not used, the SPI cable must use twisted pairs, with each SPI signal twisted with its adjacent ground signal.

All SPI connectors (P2 through P7) have the same pinout:

PIN	FUNCTION	DIR
1	+5V	FROM 7I46
2	GND	TO 7I46
3	FRAME(N)	FROM 7I46
4	GND	FROM 7I46
5	DOUT(N)	FROM7I46
6	GND	FROM 7I46
7	CLK(N)	FROM 7I46
8	GND	FROM 7I46
9	DIN(N)	TO 7I46
10	+5V	FROM 7I46

"N" is the SPI channel, the SPI connectors and channels are as follows:

SPI CONNECTOR	SPI CHANNEL
P2	0
P3	1
P4	2
P5	3
P6	4
P7	5

OPERATION

5V POWER

The 7I46 being passive requires no 5V power for operation, the SPI channels however may draw up to 500 mA of current per channel. This power will normally be supplied via TB1. For testing and with low power SPI devices, the SPI connectors can get their power from the controller cable

If W1 is on the "UP" position, the controller cable will supply the SPI connector power and T1 can remain unconnected. This mode can be used for testing but it is suggested that W1 be placed in the "DOWN" position and SPI power be supplied via TB1 for most applications.

The power from connector TB1 Passes through a 3.75A PTC device before being routed to the I/O terminals. This limits the total I/O power supplied by the 7I46 to ~3 A in 0 to 70C ambients.

Note that the 5V power supplied to the SPI connectors via TB1 is switched by a high side switch that disconnect the SPI devices power when cable power is lost. This is done to prevent back-powering the FPGA card from SPI outputs when the FPGA card is powered down.

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.75	5.25	VDC
MAXIMUM POWER TO I/O CONNECTORS	---	500	mA
Per SPI connector			
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND